U35JC SCHEMATIC Revision 1.0

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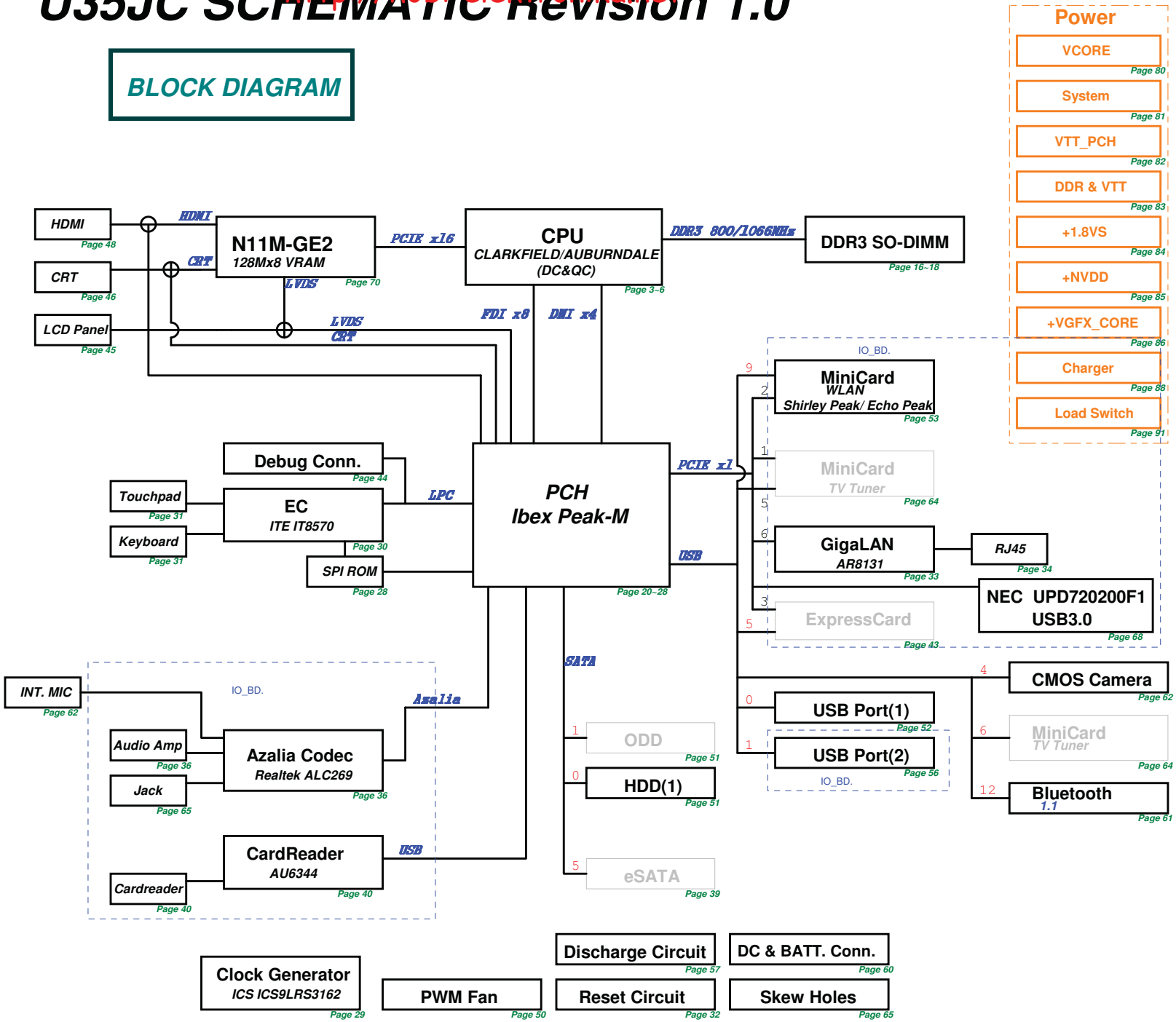
BLOCK DIAGRAM



ASUS	Title : Block Diagram
ASUSTeK COMPUTER INC. NB4	Engineer: Leon
Size C	Project Name U35JC
Rev 1.0	
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PCH_IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	Native	GPIO0	EXT PU	+3VS
GPIO 01	Native	GPIO1	INT PU, EXT PU	+3VS
GPIO [2:5]	Native	PCI_INT[E:H]#	EXT PU	+3VS
GPIO 06	GPI	DGPU_HPD_INTR#_R	INT PU, EXT PU	+3VS
GPIO 07	GPI	USB3_SMI#	INT PU, EXT PU	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	-	EXT PU	+3VSUS
GPIO 10	Native	-	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS_ORG
GPIO 12	Native	-	-	-
GPIO 13	Native	HDA_DOCK_RST#	INT PD	-
GPIO 14	Native	-	-	+3VSUS
GPIO 15	GPO	BT_LED	INT PD	-
GPIO 16	GPO	DGPU_HOLD_RST#	-	-
GPIO 17	GPI	DGPU_PWROK	EXT PD & INT PU	GND
GPIO 18	Native	CLK_REQ1_TV#	EXT PU	+3VS
GPIO 19	Native	SATA1GP	EXT PU	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PD	GND
GPIO 21	Native	SATA0GP	EXT PU	+3VS
GPIO 22	GPO	WLAN_LED	-	-
GPIO 23	Native	LPC_DRQ#1	INT PU	-
GPIO 24	GPO	USB20_SEL	-	-
GPIO 25	Native	CLKREQ3_NEWCARD#	EXT PU	+3VSUS_ORG
GPIO 26	GPI	CLKREQ4_USB	EXT PD	GND
GPIO 27	Native	VRM_EN	INT PU	-
GPIO 28	GPO	WLAN_ON#	INT PU	-
GPIO 29	Native	ME_PM_SLP_LAN#_PCH	-	-
GPIO 30	GPO	ME_SusPwrDnAck	EXT PU	+3VSUS_ORG
GPIO 31	GPI	ME_AC_PRESENT_PCH	EXT PU	+3VSUS_ORG
GPIO 32	GPI	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPI	HDA_DOCK_EN#	EXT PD, INT PU	GND
GPIO 34	Native	GPIO34	EXT PU	-
GPIO 35	Native	SATA_CLK_REQ#	EXT PD	-
GPIO 36	GPO	dGPU_PWR_EN#_GPIO36	-	-
GPIO 37	GPI	DGPU_PRSNT#	-	-
GPIO 38	GPI	PCB_ID0	EXT PD	-
GPIO 39	GPI	PCB_ID1	EXT PD	-
GPIO 40	Native	-	EXT PU	+3VSUS
GPIO 41	Native	-	EXT PU	+3VSUS
GPIO 42	Native	-	EXT PU	+3VSUS
GPIO 43	Native	-	EXT PU	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU	+3VSUS_ORG
GPIO 45	Native	CLK_REQ6#	EXT PD, INT PU	+3VSUS_ORG
GPIO 46	Native	CLK_REQ7#	EXT PU	+3VSUS_ORG
GPIO 47	Native	CLKREQ_PEG#_R	EXT PU/PD	+3VSUS_ORG
GPIO 48	Native	GPIO48	EXT PU	+3VS
GPIO 49	GPO	PCH_TEMP_ALERT#	EXT PU	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU	+3VS
GPIO 51	Native	PCI_GNT1#	INT PU	-
GPIO 52	GPO	dGPU_SELECT#_GPIO52	-	+3VS
GPIO 53	Native	-	INT PU	-
GPIO 54	Native	PCI_REQ3#	EXT PU	+3VS
GPIO 55	Native	PCI_GNT3#	EXT PU, INT PU	+3VS
GPIO 56	Native	CLKREQ_GLAN#	EXT PD	GND
GPIO 57	GPO	BT_ON	-	-
GPIO 58	GPI	SML1_CLK	EXT PU	+3VSUS_ORG
GPIO 59	Native	-	EXT PU (Not used)	+3VSUS
GPIO 60	Native	SML0ALERT#	EXT PU	+3VSUS_ORG
GPIO 61	Native	PM_SUS_STAT#	-	-
GPIO 62	Native	SUS_CLK	-	-
GPIO 63	Native	SLP_S5#	-	-
GPIO 64	Native	CLK_OUT0	INT PD	-
GPIO 65	Native	CLK_OUT1	INT PD	-
GPIO 66	GPO	CLK_OUT2	INT PD	-
GPIO 67	GPO	CLK_OUT3	-	-
GPIO 72	Native	PW_BATLOW#	EXT PU, INT PU	+3VSUS_ORG
GPIO 73	Native	CLK_REQ0#	INT PU	+3VSUS_ORG
GPIO 74	Native	SML1ALERT#	EXT PU	+3VSUS_ORG
GPIO 75	GPI	SML1_DAT	EXT PU	+3VSUS_ORG

EC IT8570

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2	O	CHG_FULL_LED#
GPA3		-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN_PWM
GPA6		-
GPA7		-
GPB0	O	BATSEL_0
GPB1	O	BATSEL_1
GPB2		ME_AC_PRESENT_EC
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RCIN#
GPB7	O	PM_RSMRST#
GPC0	O	Clock_select_uc
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7	I	HDMI_HP_EC
GPE0		-
GPE1		-
GPE2		-
GPE3		-
GPE4	I	PWR_SW#
GPE5		-
GPE6	I	LID_SW#
GPE7	I	MARATHON#
GPF0	O	-
GPF1	O	VSUS_ON
GPF2	O	VCCP_DV0
GPF3	O	VCCP_DV1
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7	I	PCH_SPI_OV
GPG0	I	ME_SusPwrDnAck_EC
GPG1	I	PM_SUSB#
GPG2		-
GPG6		-
GPH0	IO	PM_CLKRUN#
GPH1	O	GFX_VR_ON
GPH2	O	CHG_EN
GPH3	O	SUSC_EC#
GPH4	O	SUSB_EC#
GPH5	O	NUM_LED#
GPH6	O	CAP_LED#
GPI0	I	VGA_ALERT#
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ALERT#
GPI5	I	CPU_ISENSE
GPI6	I	GPU_ISENSE
GPI7	I	VCORE_CMSET
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISET_EC
GPJ4	O	CPU_DV0
GPJ5	O	CPU_DV1

PCIE 1	
PCIE 2	Minicard WLAN
PCIE 3	
PCIE 4	USB 3.0
PCIE 5	
PCIE 6	GLAN
PCIE 7	
PCIE 8	

SATA 0	SATA HDD (1)
SATA1	
SATA4	
SATA5	

USB 0	USB Port (1)
USB 1	Card Reader(2.0)
USB 2	USB Port (3)
USB 3	
USB 4	
USB 5	
USB 6	
USB 7	
USB 8	WiFi/WiMax
USB 9	Camera
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
Clock Generator(ICS9LVS3162BKLFT)	1101001x (D2)	
SO-DIMM 0	1010000x (A0)	
SO-DIMM 1	1010001x (A2)	
WiFi/WiMax	N/A	
EC Master (SMB1)		
SM-Bus Device	**SM-Bus Address**	
INA219AIDCNR(CPU)	x1000000 (40)	
INA219AIDCNR(VGA)	x1000001 (41)	

Device Identification

	CPU Thermal Sensor P/N:	component name
1st	06G073050010	Current/Power Monitor
S		
S		
S		

	Clock Gen P/N:	component name
1st	06G011604010	ICS9LRS3197
S		
S		

ASUSTeK COMPUTER INC. NB4

Title : System Setting

Engineer: Leon

Size	Project Name	Rev
C	U35JC	1.0

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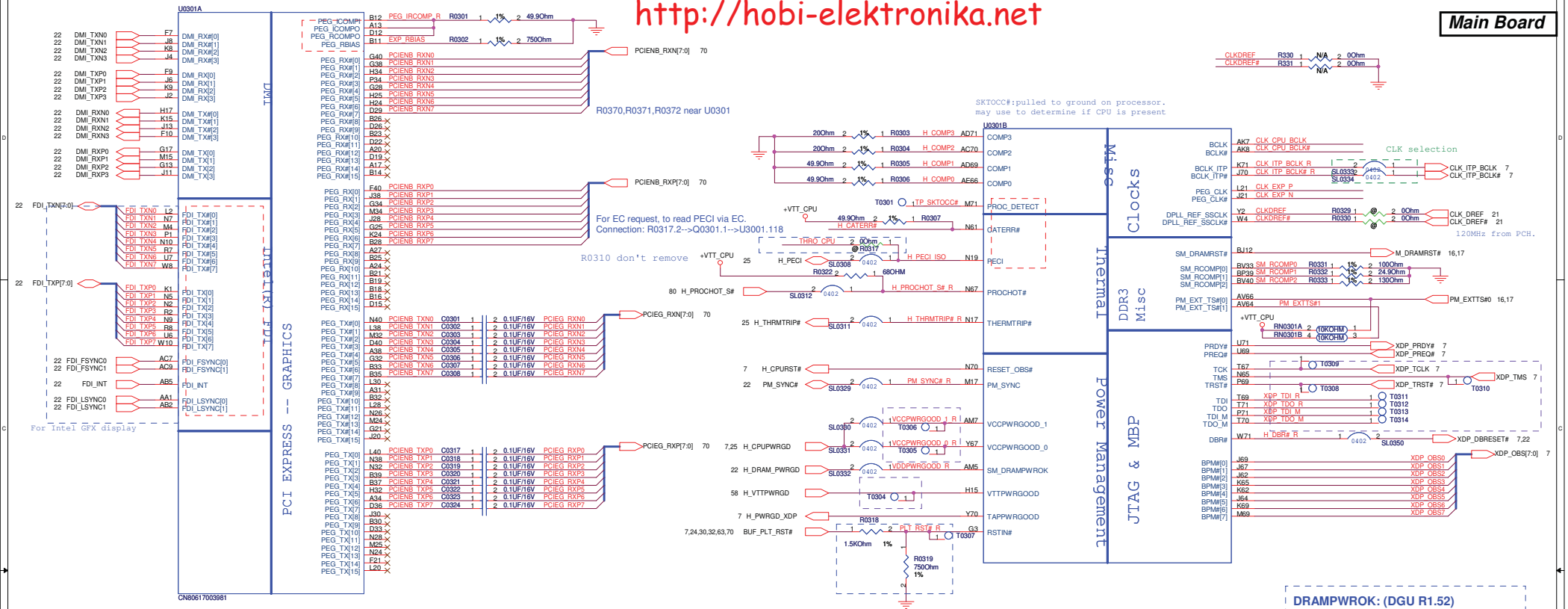
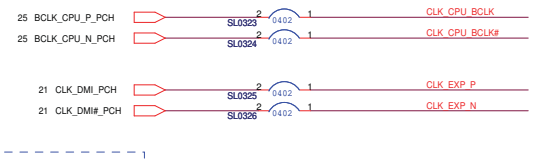
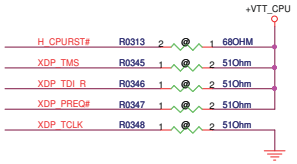
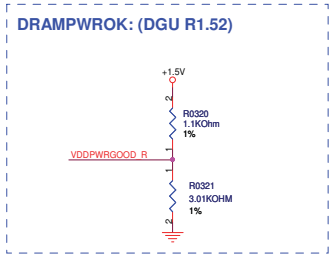
Main Board



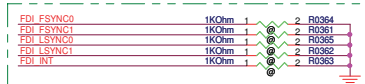






FDI disable: (For discrete graphic)

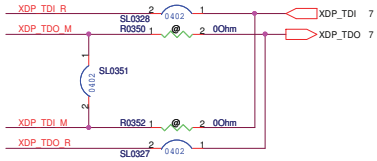
1. **NC:**
   FDI_TX#[0:7],FDI_TX[0:7],FDI_RX#[0:7],FDI_RX[0:7]
   VCC_AXGSENSE,VSS_AXGSENSE
2. **Pull-down to GND via 1KΩ ± 5% resistor:**
   FDI_FSYNC[0:1],FDI_LSYNC[0:1],FDI_INT,GFX_IMON
   ~15mW power saving.(DG R0.8 P.70)
3. **Connected to GND:**
   VCCAXG,
4. **Can be connected to GND directly:**
   DPLL_REF_CLK,DPLL_REF_CLK#
5. **Connect to +V1.05S rail:**
   VCCFDIPLL

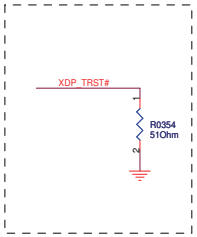


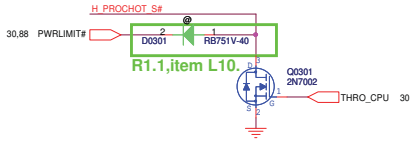
DG R1.1 P.83:

FDI_FSYNC[0],FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1] can be ganged together with one resistor.
On the other hand,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on PCH side can be left as no connect without any power or functional impact.

JTAG MAPPING







Add test point for factory ICT boundary scan .

CPU: (page3)

Ball#	Signal	Test Point
	BCLK	T0303
	VTTPWRGOOD	T0304
	VCCPWRGOOD_0	T0305
	VCCPWRGOOD_1	T0306
	RSTIN#	T0307
	TRST#	T0308
	TCK	T0309
	TMS	T0310
	TDI	T0311
	TDO	T0312
	TDI_M	T0313
	TDO_M	T0314

PCH: (page 20,21,22)

Ball#	Signal	Test Point
	JTAG_TCK	T2013
	JTAG_TMS	T2014
	JTAG_TDI	T2015
	JTAG_TDO	T2016
	JTAG_RST#	T2017
	RSMRST#	T2209
	RTCRST#	T2018
	PWROK	T2210
	MEPWROK	T2211
	LAN_RST#	T2212
	CLKIN_PCILOOPBACK	T2113
	INTVRMEN	T2019
	SYS_PWROK	T2213
	SRTCRST#	T2020

ASUSTeK COMPUTER INC. NB1

Title : CPU(1)_DMI,PEG,FDI,CLK,MISC

Engineer: Leon

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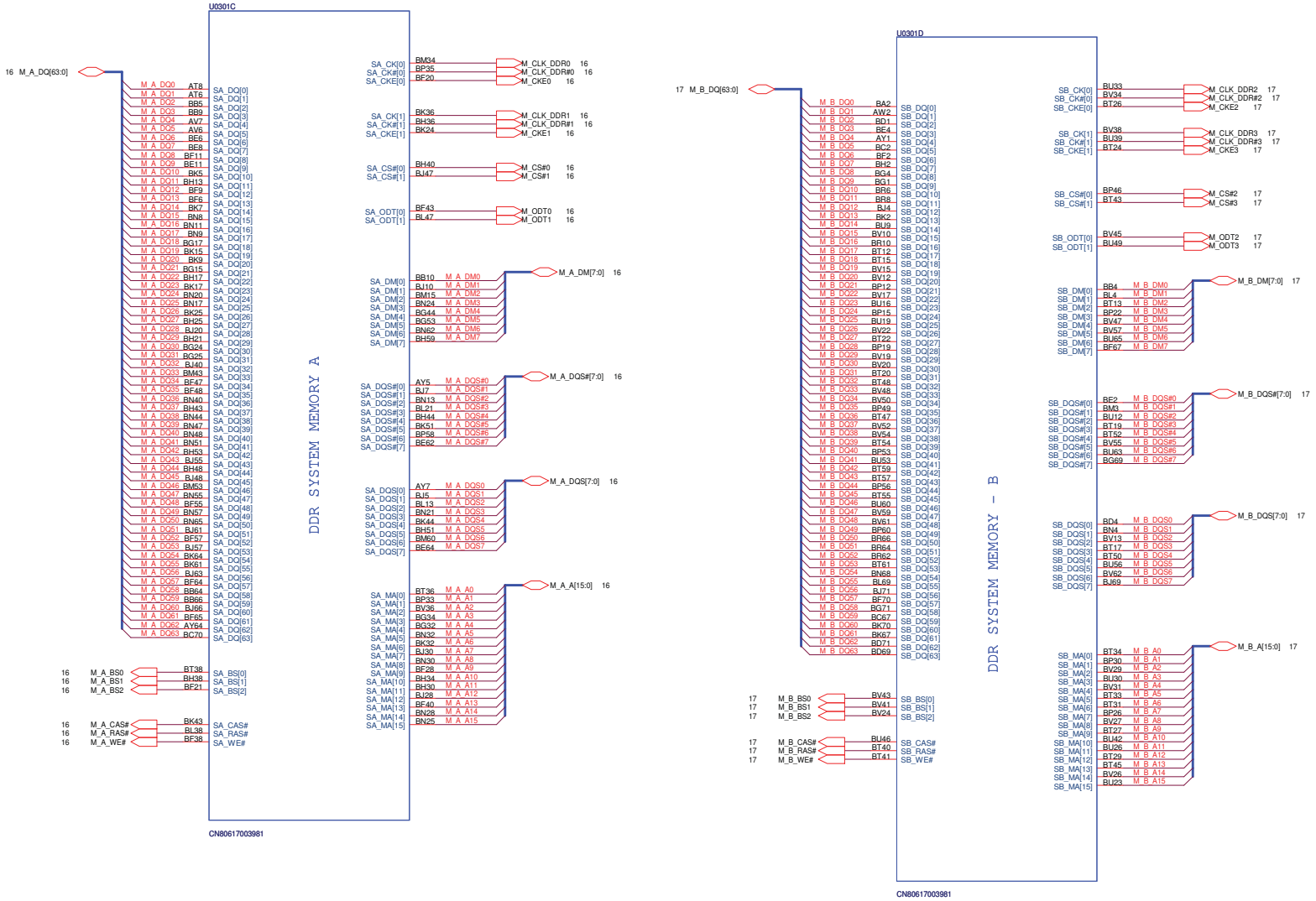

ASUS	Title : CPU(2)_DDR3	
ASUSTeK COMPUTER INC. NB1	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
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CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)
- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

CFG[3]: PCIE Static Numbering Lane Reversal.(Auburndale Only)
- 1:Normal Operation (Default)
- 0:Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

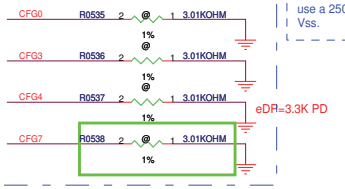
CFG[4]: Embedded DisplayPort Detection.(Auburndale Only)
- 1:Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0:Enabled - An external Display Port device is connected to the Embedded Display Port

CFG[7]: Fixed for PCI Express 2.0 jitter specifications.(Clarksfield)
Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor
For a common motherboard design (for AUB and CFD),
the pull-down resistor should be used. Does not impact AUB functionality.
Unmount if Intel has fixed this issue.

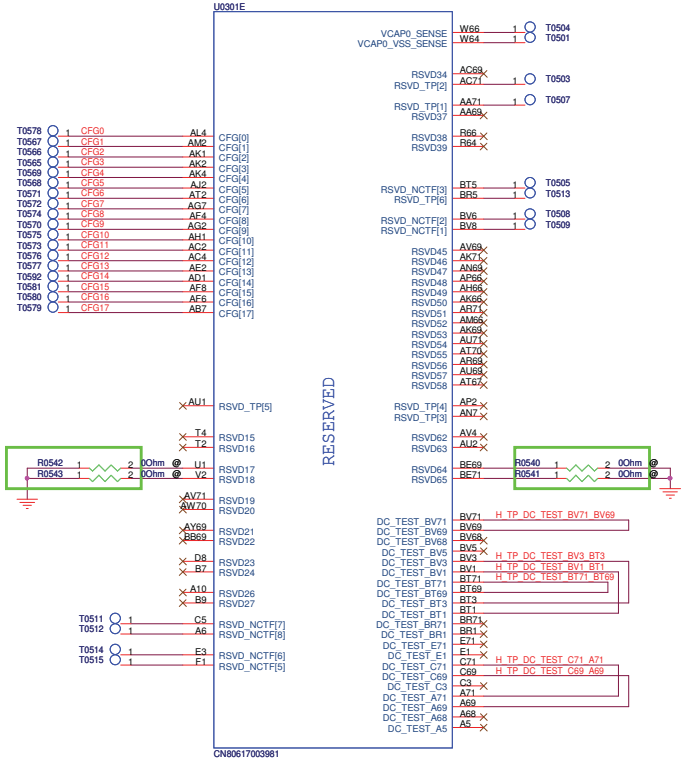
Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

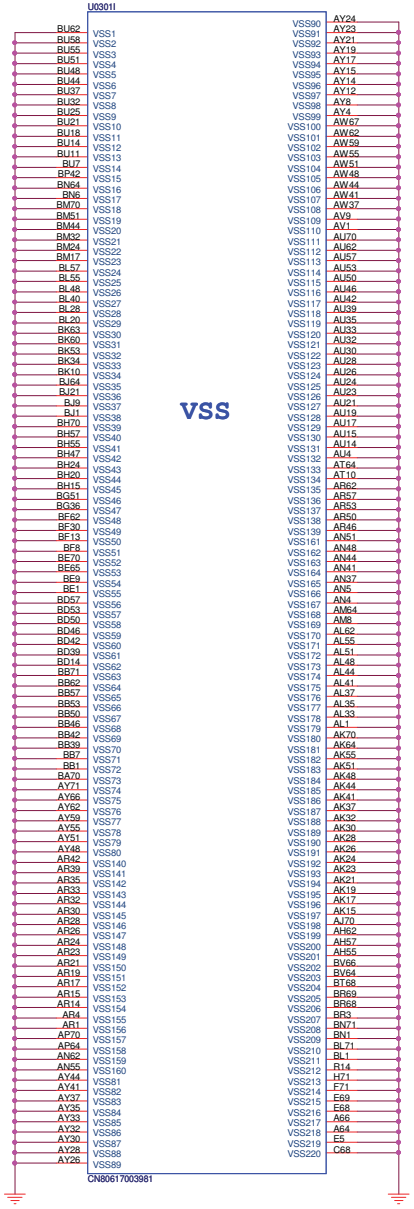
Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.

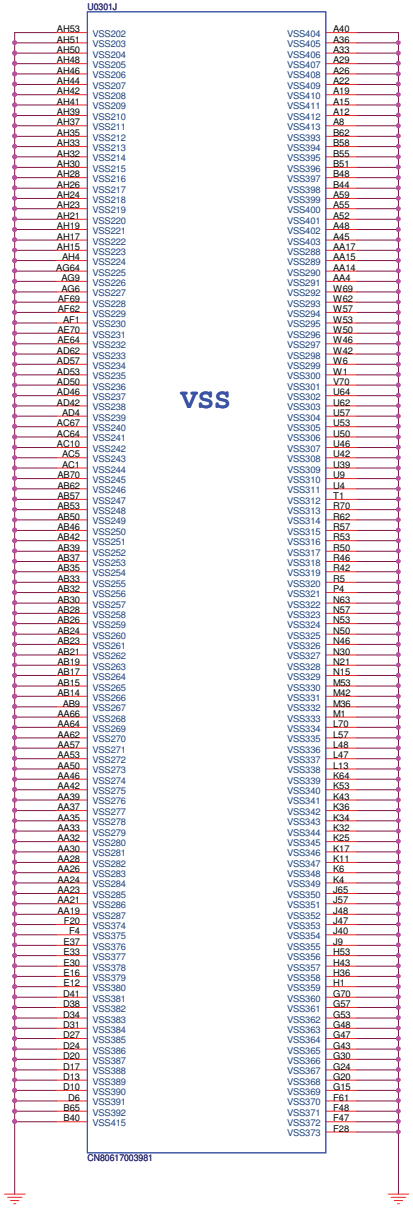
Intel sighting #: 402607(3393727)
To drive a value of zero on CFG[0] pin use a 250 Ohm pull down resistor to Vss.



R1.1,item B1







ASUSTeK COMPUTER INC. NB1	Title : CPU(3)_CFG,RSVD,GND		
	Engineer: Leon		
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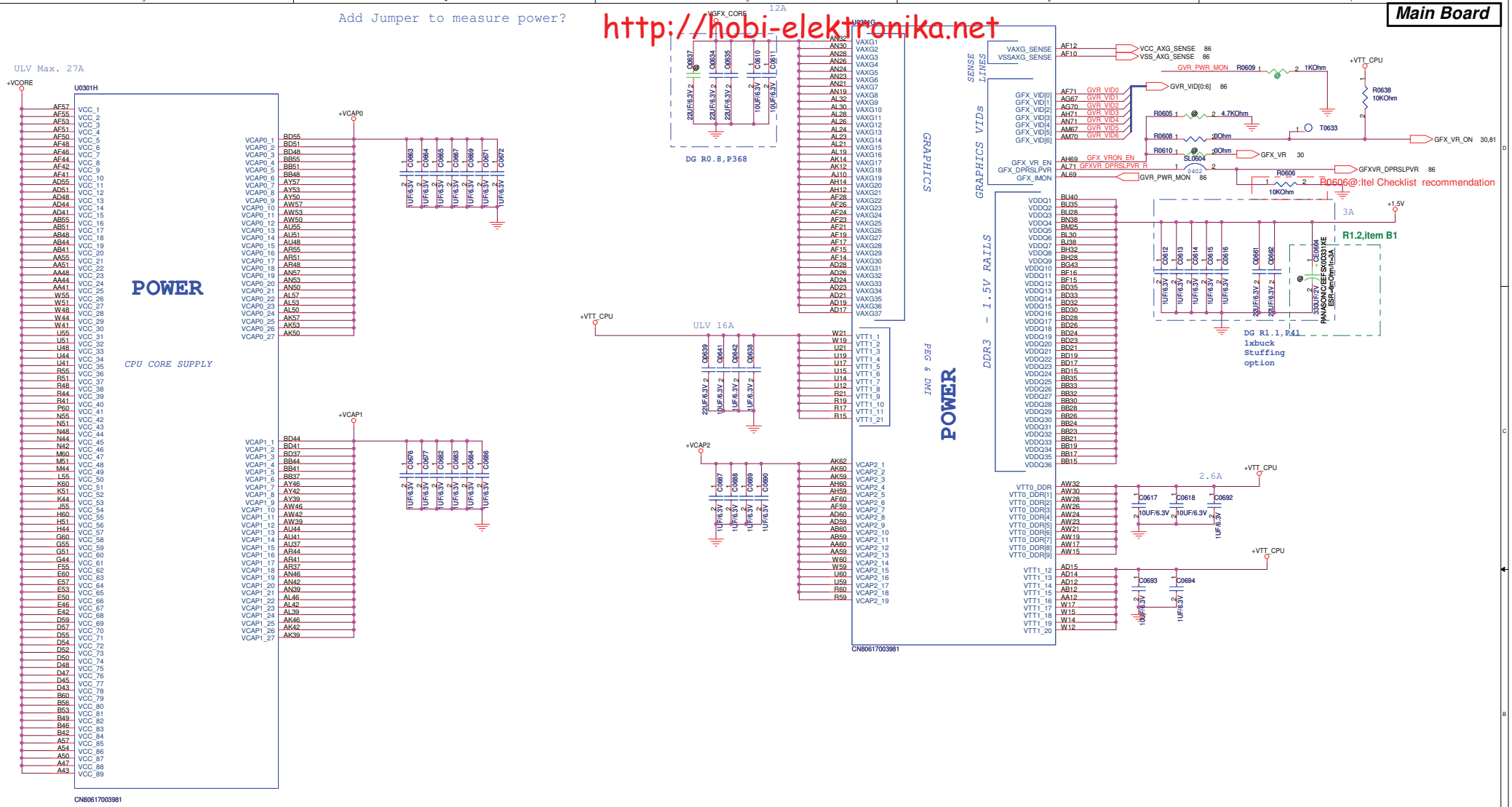

ASUSTeK COMPUTER INC. NB1	Title : CPU(4)_PWR		
	Engineer: Leon		
Size C	Project Name U35JC		Rev 1.0
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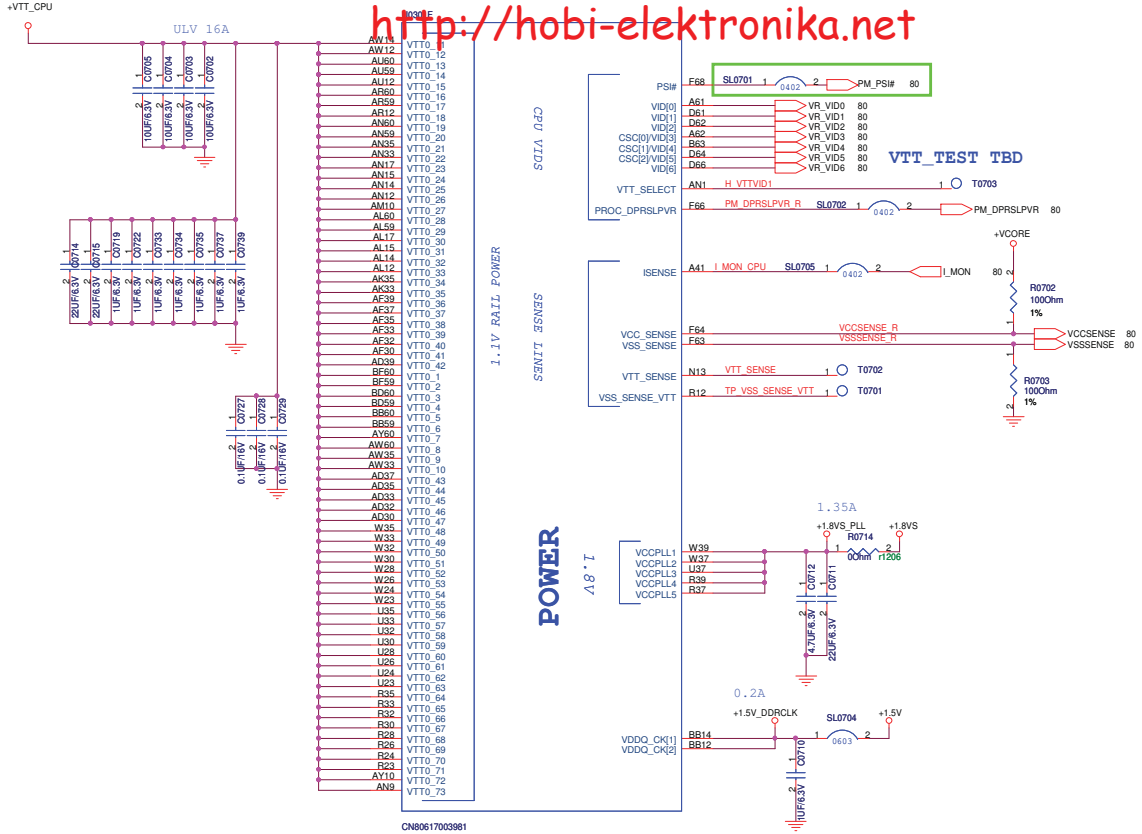

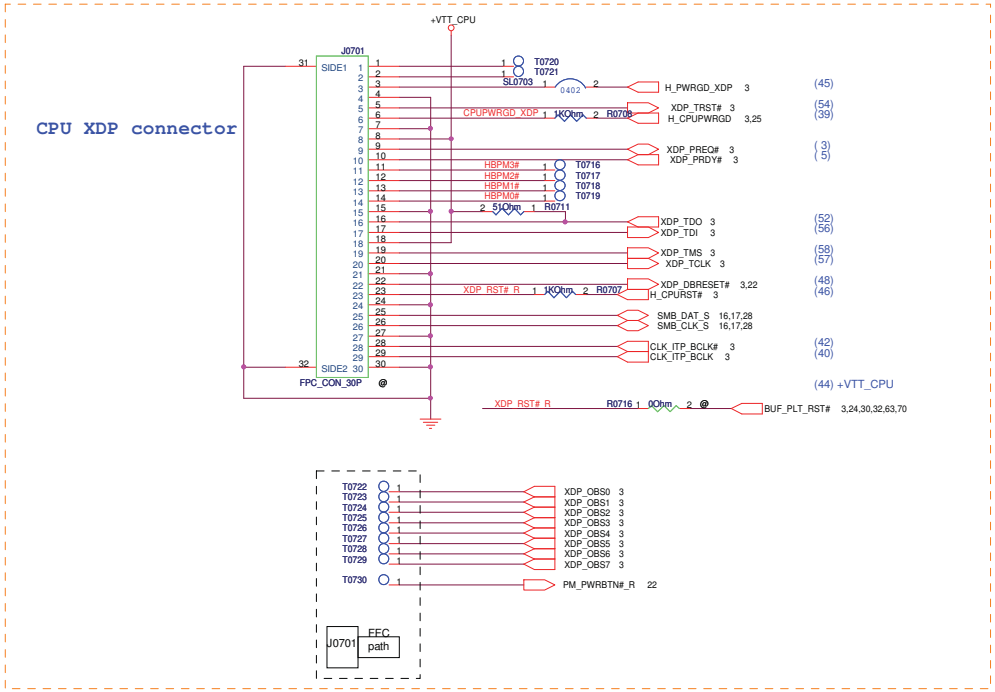

Put these test point near J0701
Put it away from the FFC path.

ASUSTeK COMPUTER INC. NB1	Title : CPU(5)_PWR & XDP	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
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ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: Leon		
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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: *Leon*		
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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: *Leon*		
Size: Custom	Project Name: U35JC		Rev: 1.0
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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: *Leon*		
Size: Custom	Project Name: U35JC		Rev: 1.0
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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: *Leon*		
Size: Custom	Project Name: U35JC		Rev: 1.0
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Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: *Leon*		
Size: Custom	Project Name: U35JC		Rev: 1.0
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ASUS	Title :	
ASUSTeK COMPUTER INC. NB6	Engineer: Leon	
Size: A	Project Name: U35JC	Rev: 1.0
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ASUS	Title :	
ASUSTeK COMPUTER INC. NB6	Engineer: Leon	
Size: A	Project Name: U35JC	Rev: 1.0
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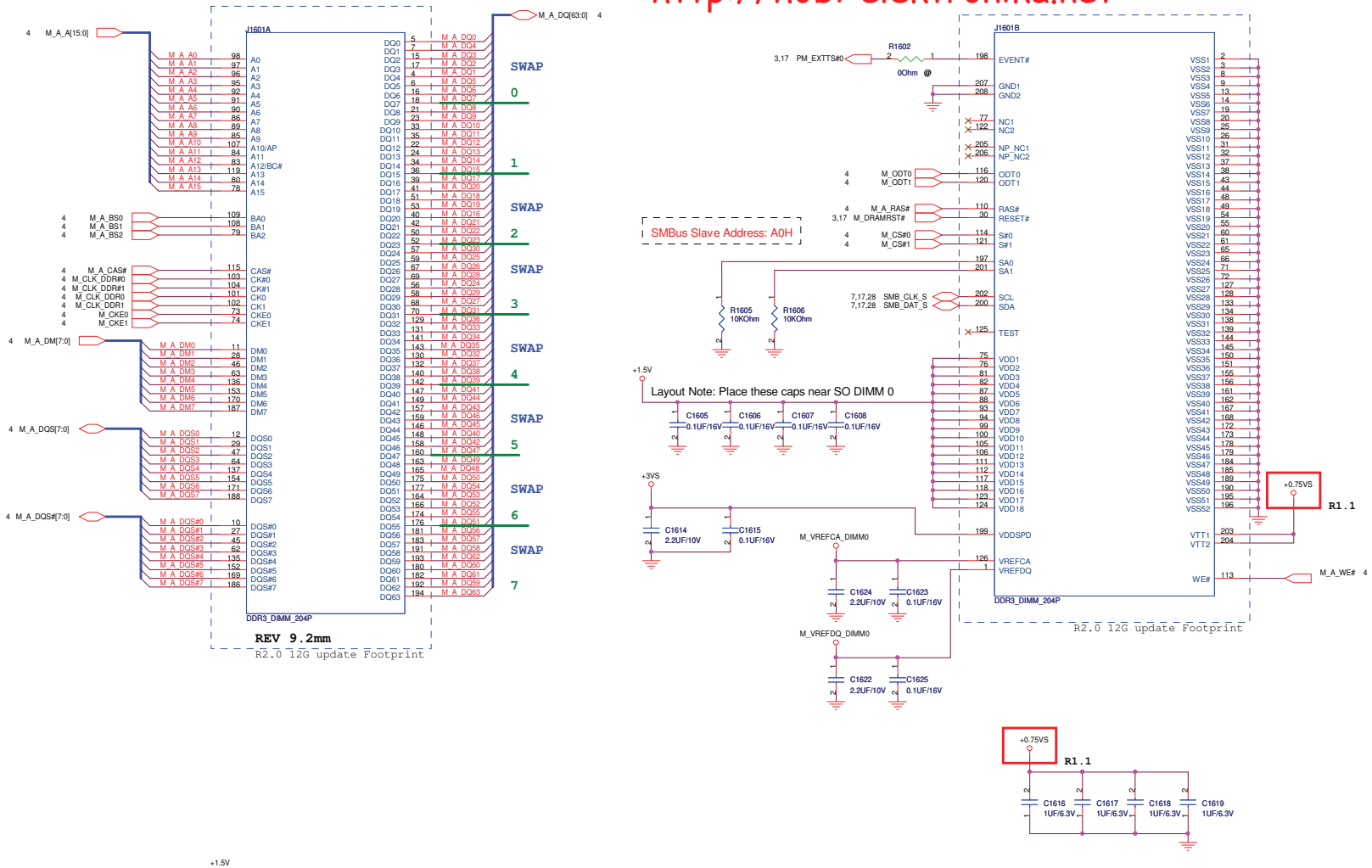
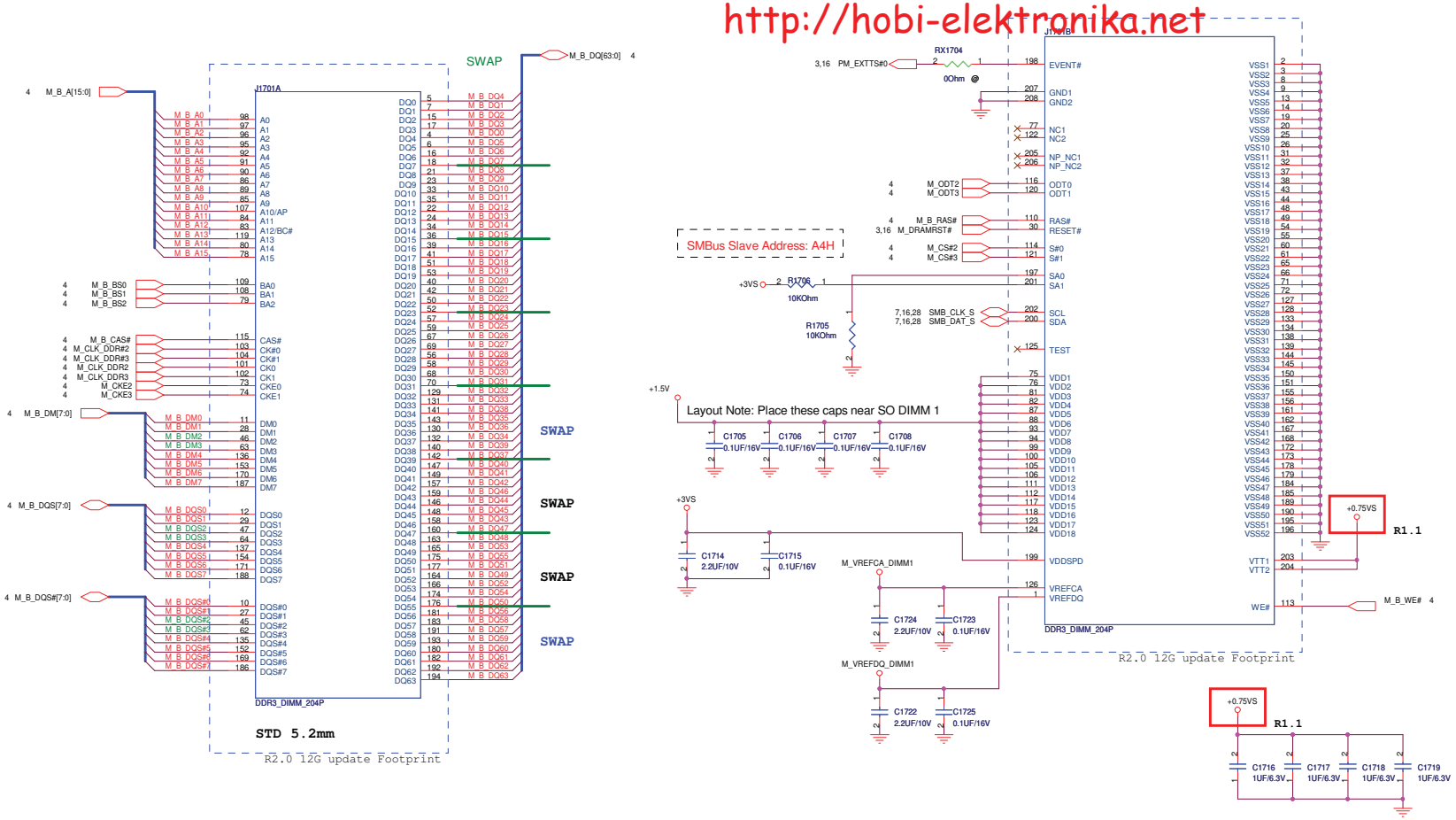
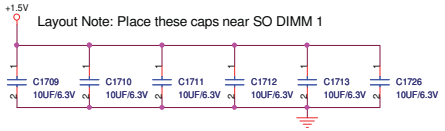


ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_0	Engineer: Leon
Size C	Project Name U35JC	Rev 1.0
Date: Friday, April 09, 2010	Sheet 16 of 99	

http://hobi-elektronika.net





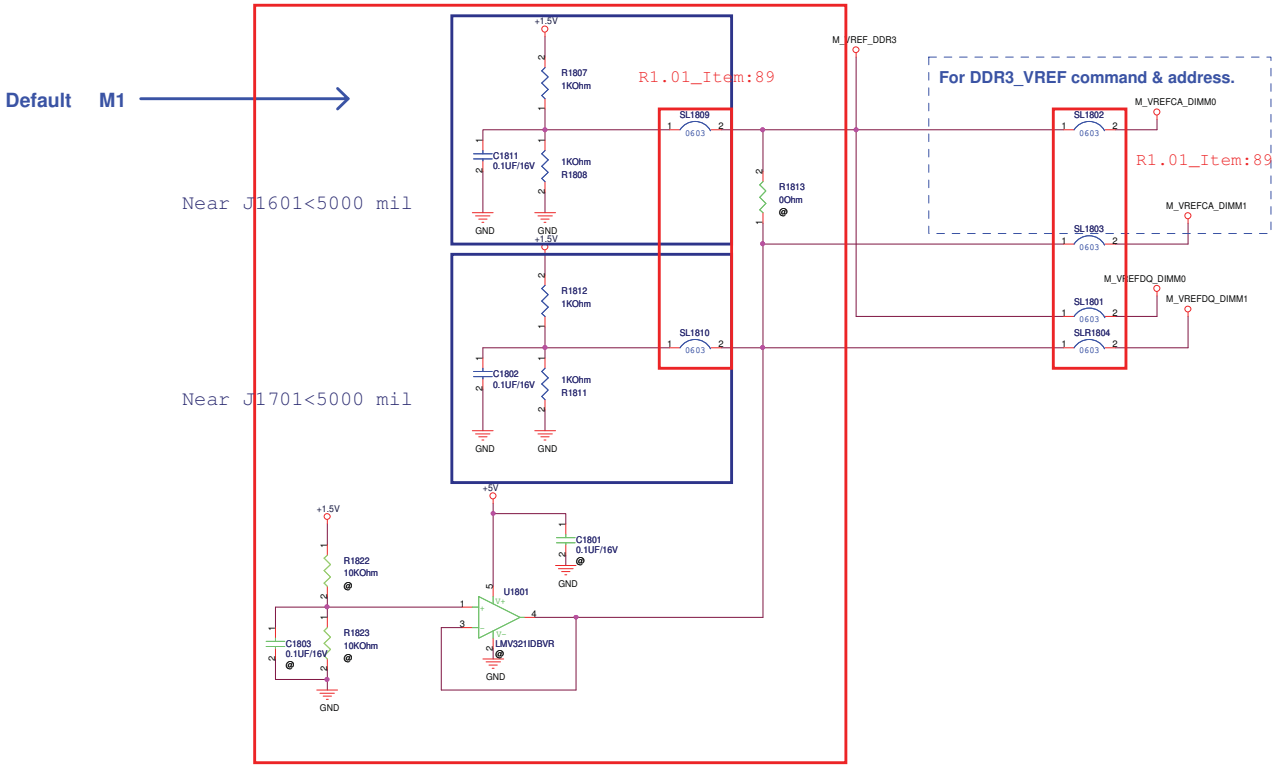
ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_1		
	Engineer: Leon		
Size C	Project Name U35JC		Rev 1.0
Date: Friday, April 09, 2010	Sheet 17 of 99		

http://hobi-elektronika.net

Calpella Clarksfield DDR3 SO-DIMM VREFDQ
Platform Design Guide Change Details

DDR3 Vref

Intel Document Number: 400755

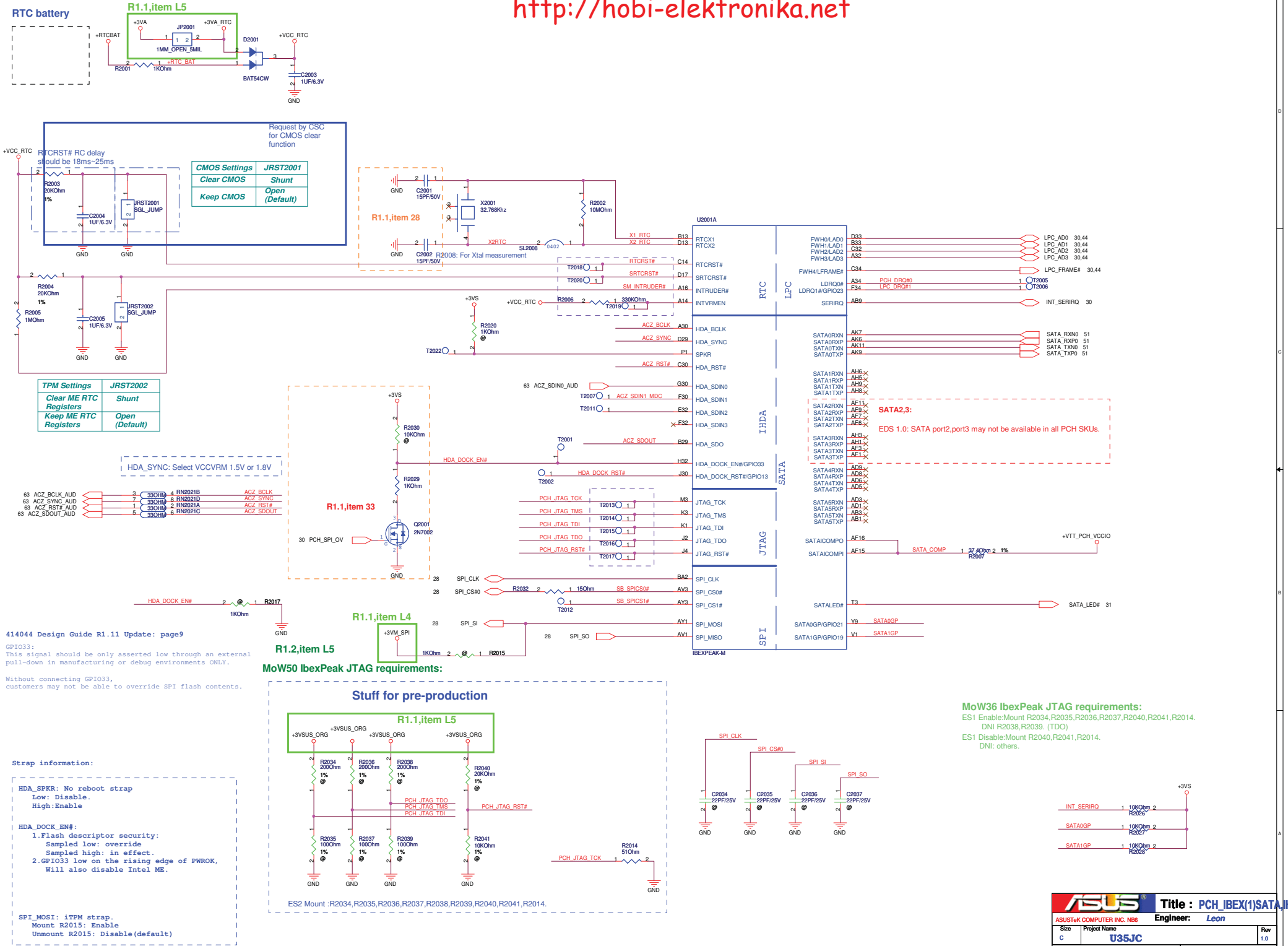


ASUSTeK COMPUTER INC. NB6	Title DDR3 CA_DQ VOLTAGE	Engineer: Leon
Size C	Project Name U35JC	Rev 1.0
Date: Tuesday, March 02, 2010	Sheet 18 of 99	

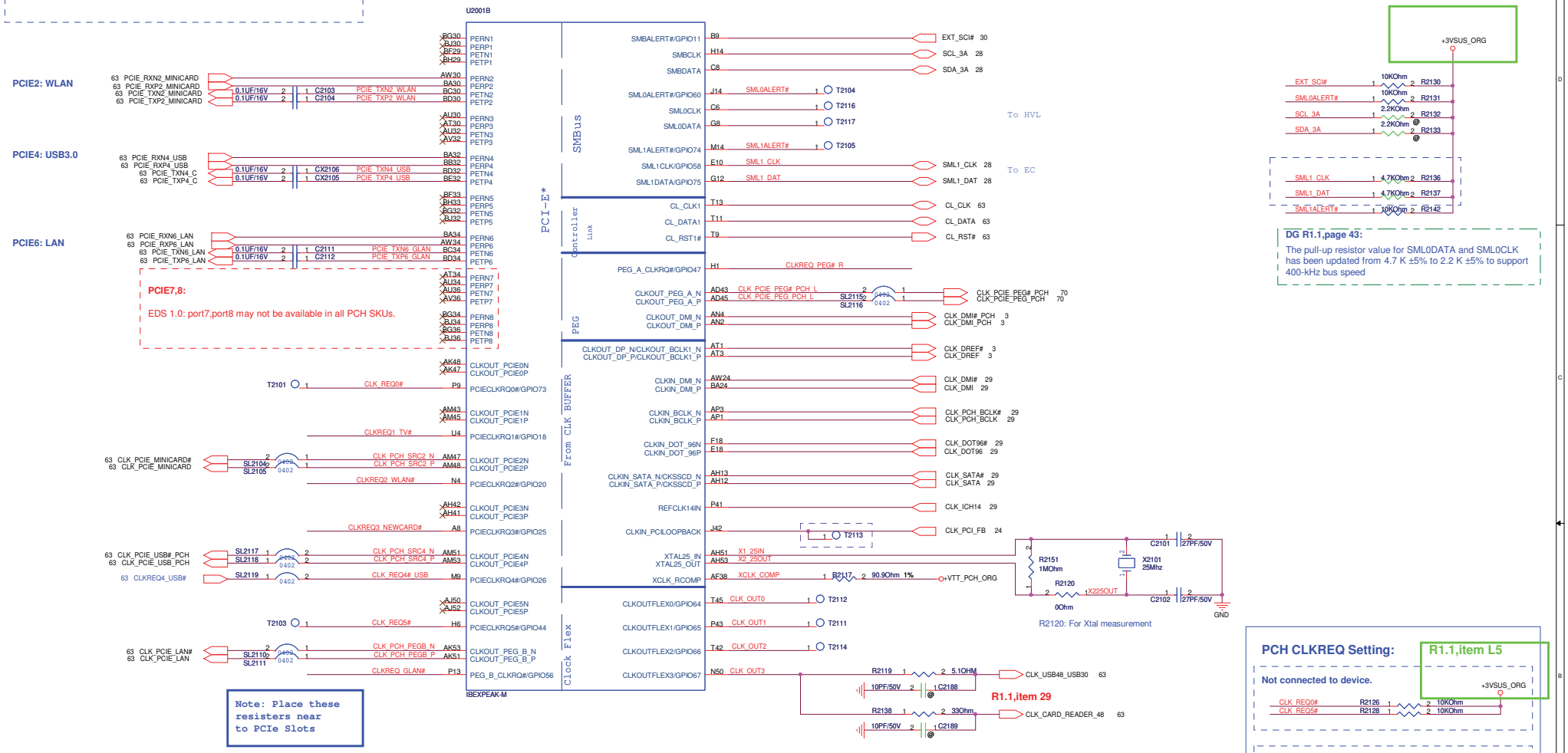
http://hobi-elektronika.net

ASUSTeK COMPUTER INC. NB1	Title :	Engineer: Wendell_lo	
Size: Custom	Project Name: U35JC		Rev: 1.0
Date: Tuesday, March 02, 2010	Sheet 19 of 99		

http://hobi-elektronika.net



http://hobi-elektronika.net



ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(2)_PCIE,CLK,SMB,PEG
	Engineer: Leon
Size C	Project Name U35JC
Rev 1.0	
Date: Friday, April 09, 2010	Sheet 21 of 99

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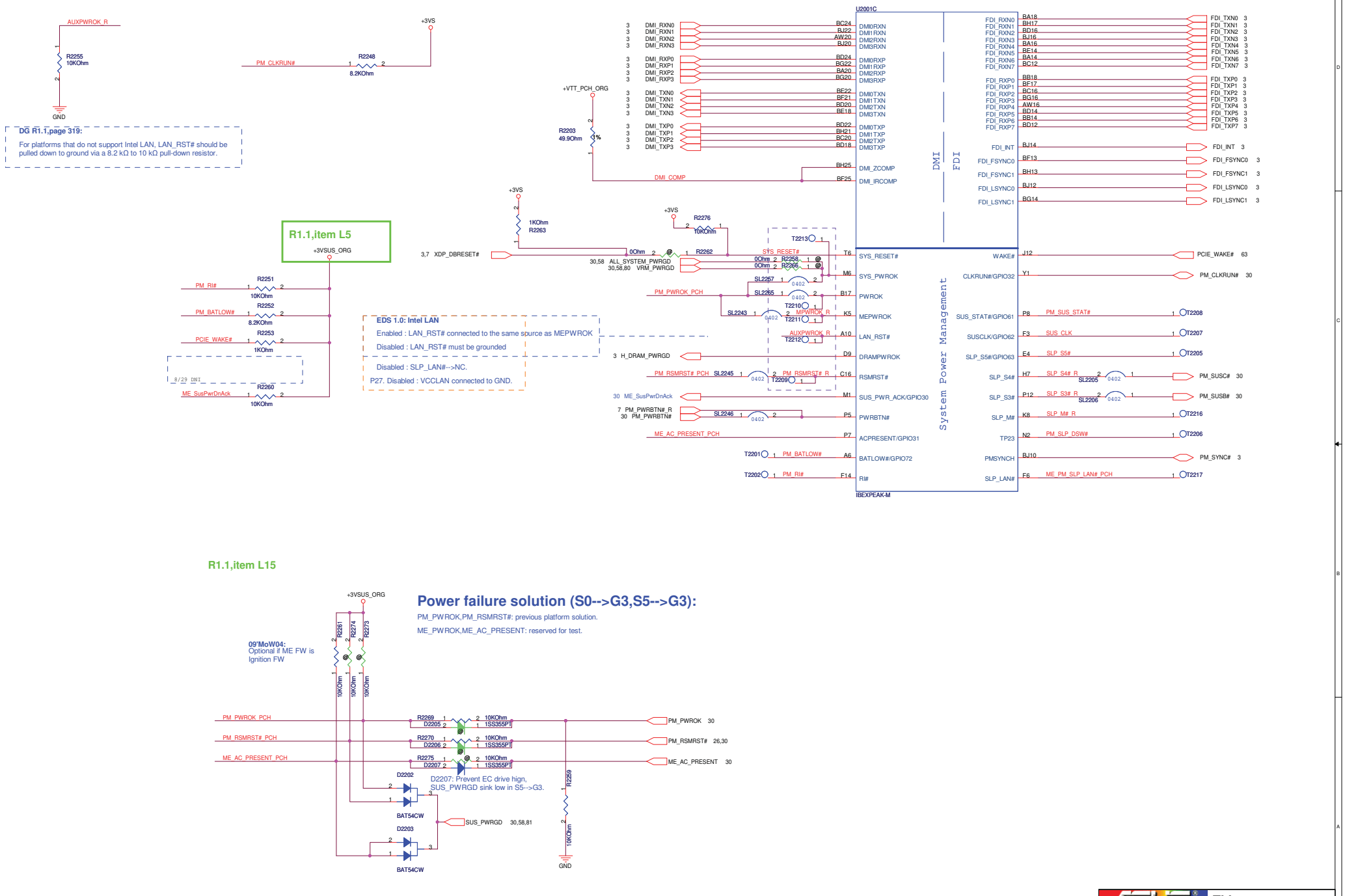
pre-ES1 not support
Reversal Feature



ASUS	Title : PCH_IBEX(3)_FDI,DMI,SYS PWR	
ASUSTeK COMPUTER INC. NB6	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
Date: Friday, April 09, 2010	Sheet 22 of 99	

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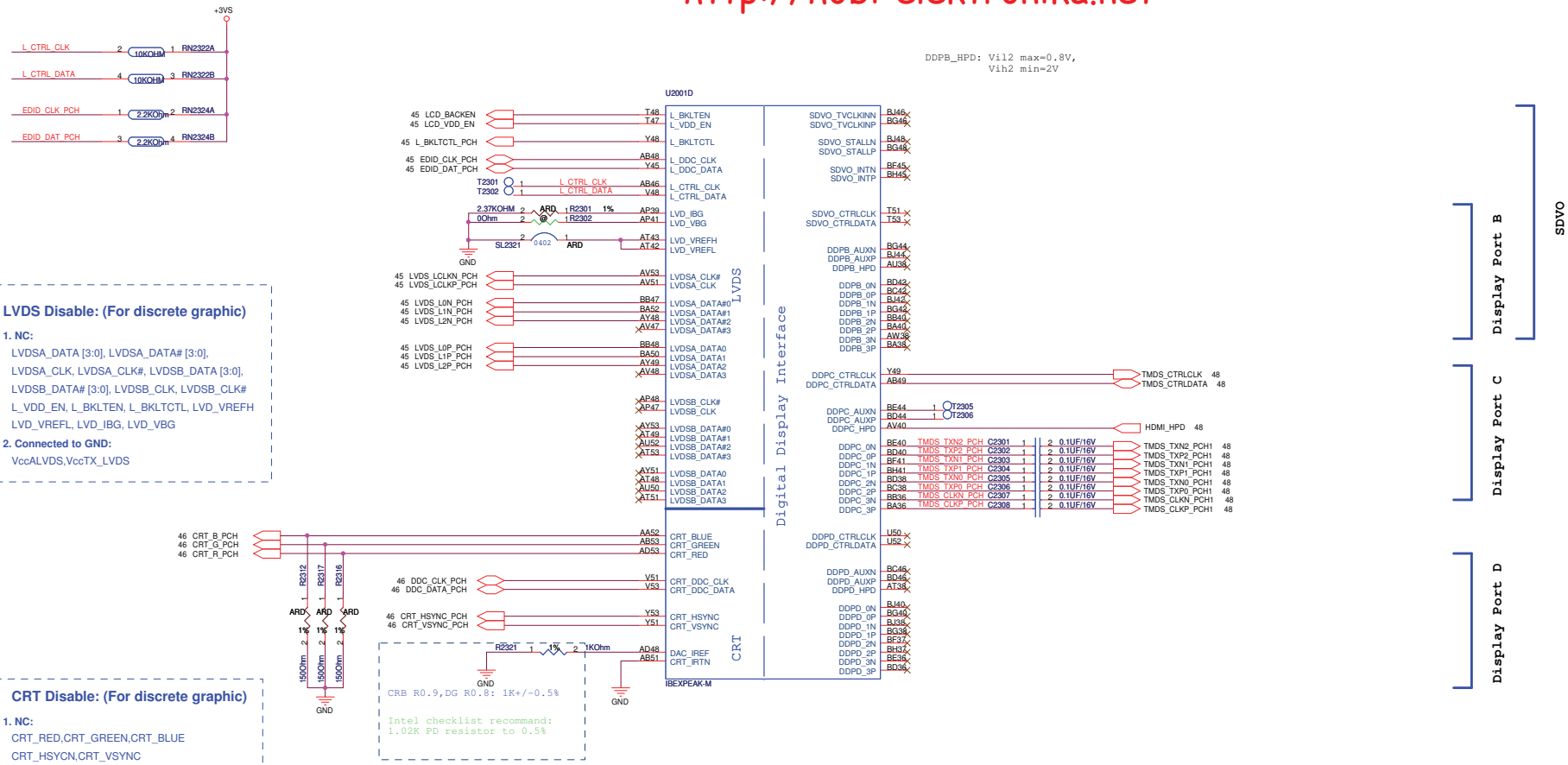


LVDS Disable: (For discrete graphic)

1. NC:
   LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
   LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
   LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
   L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
   LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
   VccALVDS,VccTX_LVDS

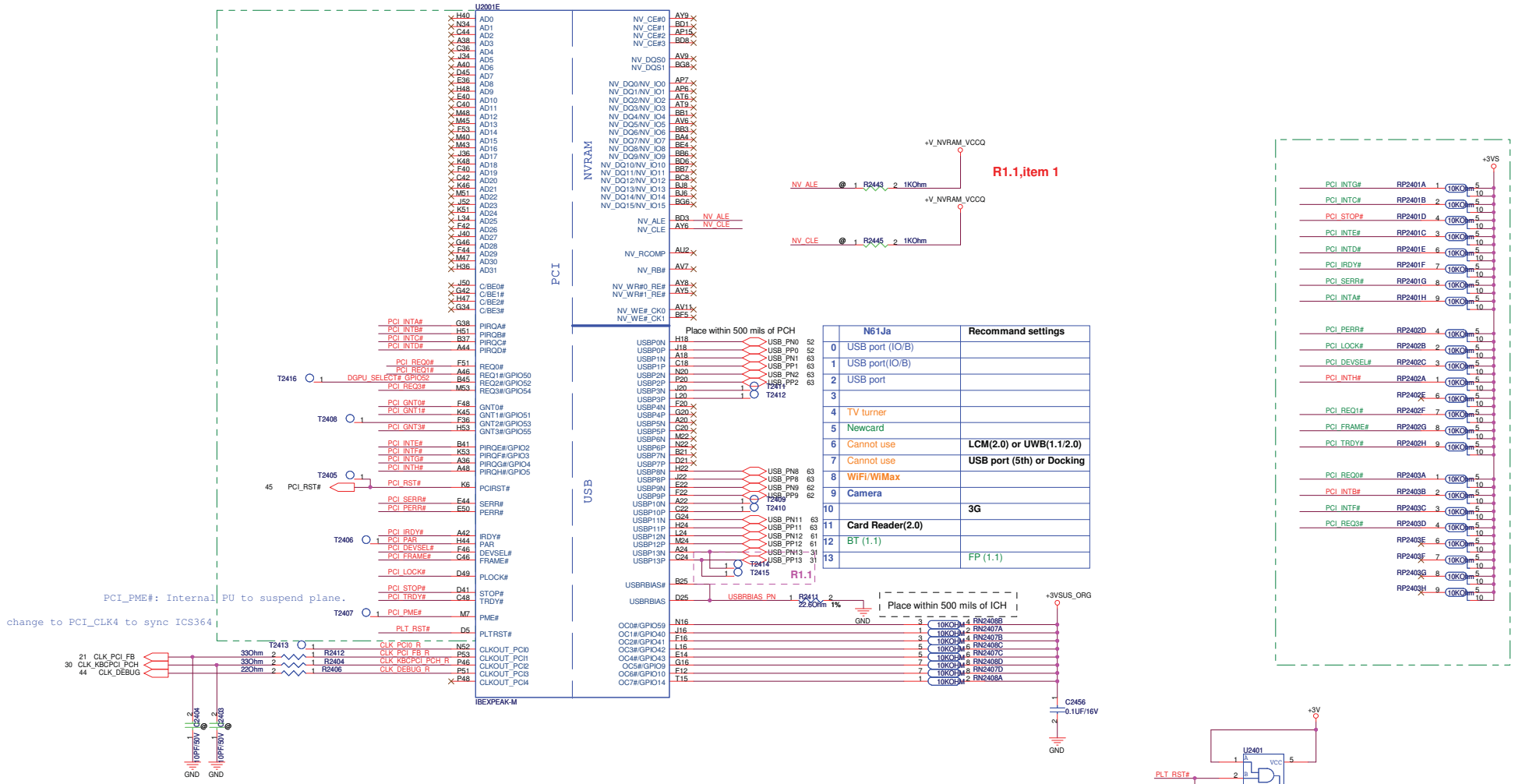
CRT Disable: (For discrete graphic)

1. NC:
   CRT_RED,CRT_GREEN,CRT_BLUE
   CRT_HSYCN,CRT_VSYNC
2. 1-kΩ ±0.5% pull-down to GND:
   DAC_IREF
3. Connected to GND:
   CRT_ITRN
4. Connect to +V3.3:
   VCCADAC

Design guide 1.62 updated: DAC_IREF CFD: 1Kohm/5% ; ARD:1Kohm/0.5%
整合料件改為1%

ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(4)_DP,LVDS,CRT		
	Engineer: Leon		
Size: C	Project Name: U35JC		Rev: 1.0
Date: Friday, April 09, 2010	Sheet 23 of 99		

http://hobi-elektronika.net



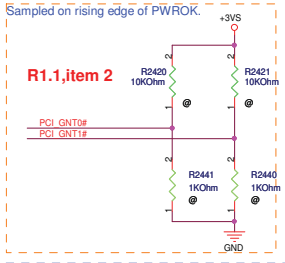
	N61Ja	Recommand settings
0	USB port (IO/B)	
1	USB port(IO/B)	
2	USB port	
3		
4	TV turner	
5	Newcard	
6	Cannot use	LCM(2.0) or UWB(1.1/2.0)
7	Cannot use	USB port (5th) or Docking
8	WiFi/WiMax	
9	Camera	
10		3G
11	Card Reader(2.0)	
12	BT (1.1)	
13		FP (1.1)

GNT0#,GNT1#: Boot BIOS Strap.

Boot BIOS Strap

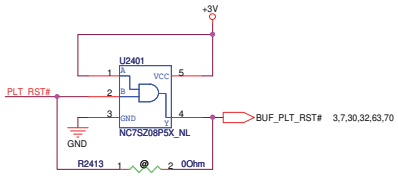
PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI **(PCH)**

Sampled on rising edge of PWROK.



GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default



ASUSTeK COMPUTER INC. NB6

Title : PCH_IBEX(5)_PCI,NVRAM,USB

Engineer: Leon

Size	Project Name	Rev
C	U35JC	1.0

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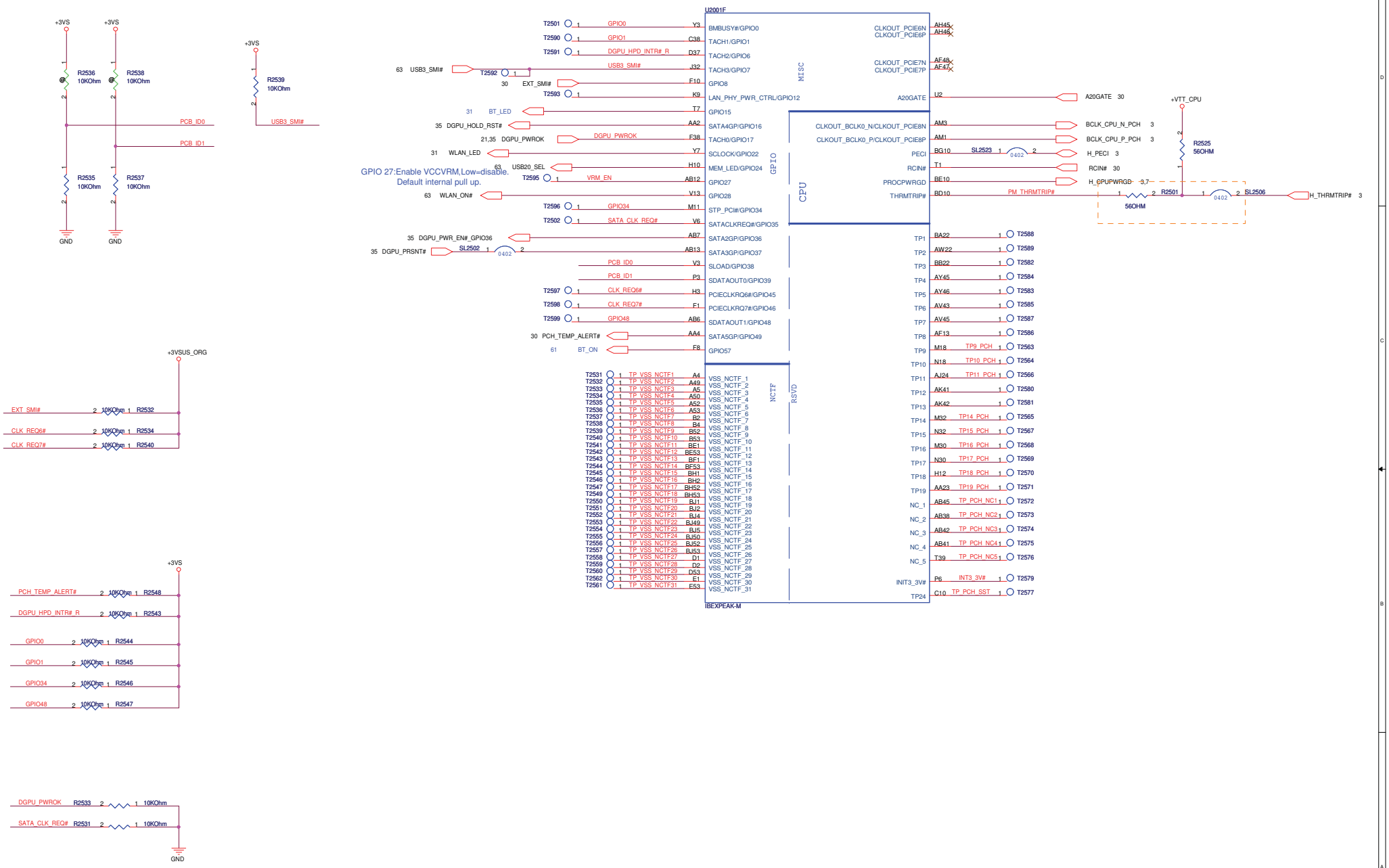
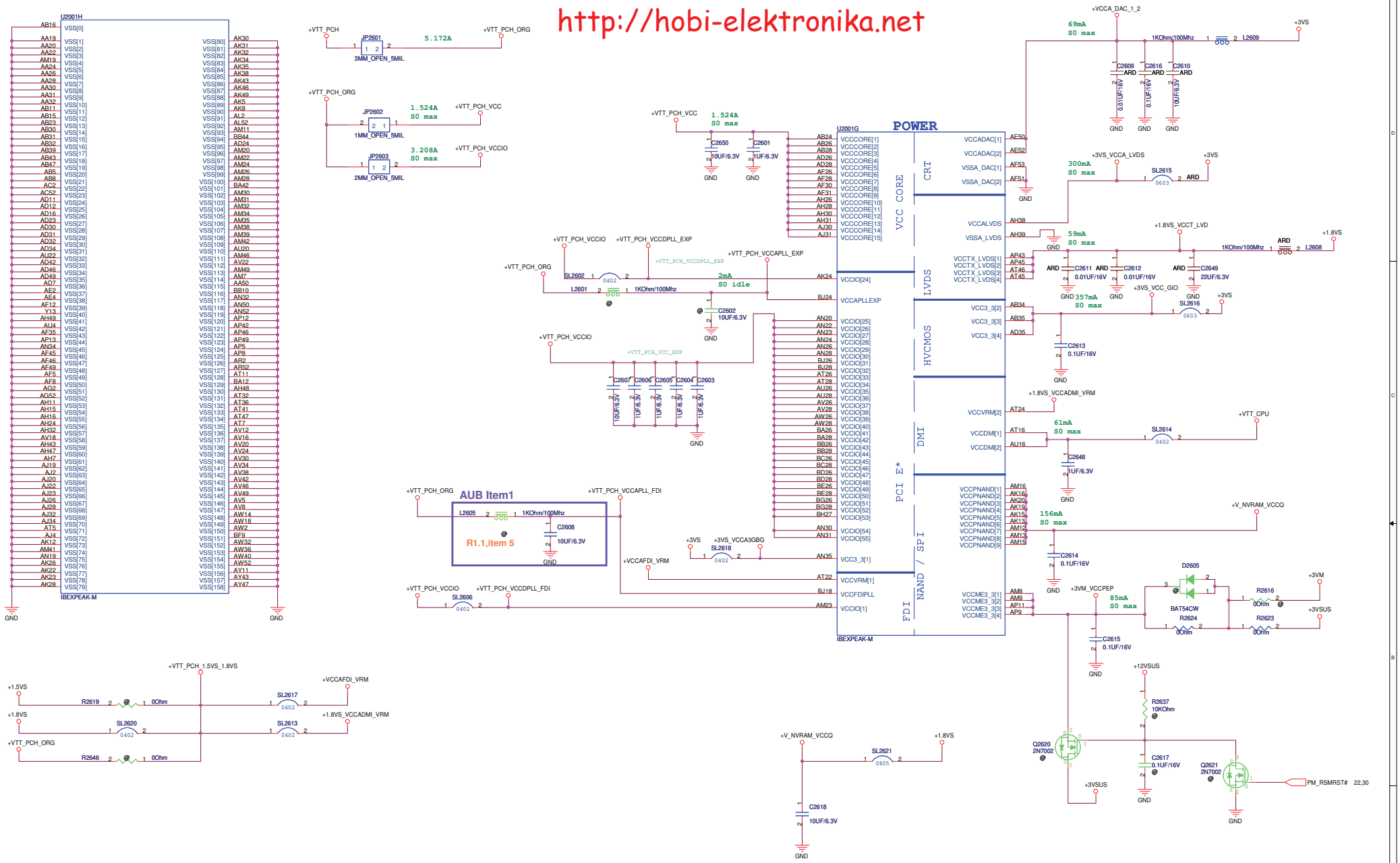


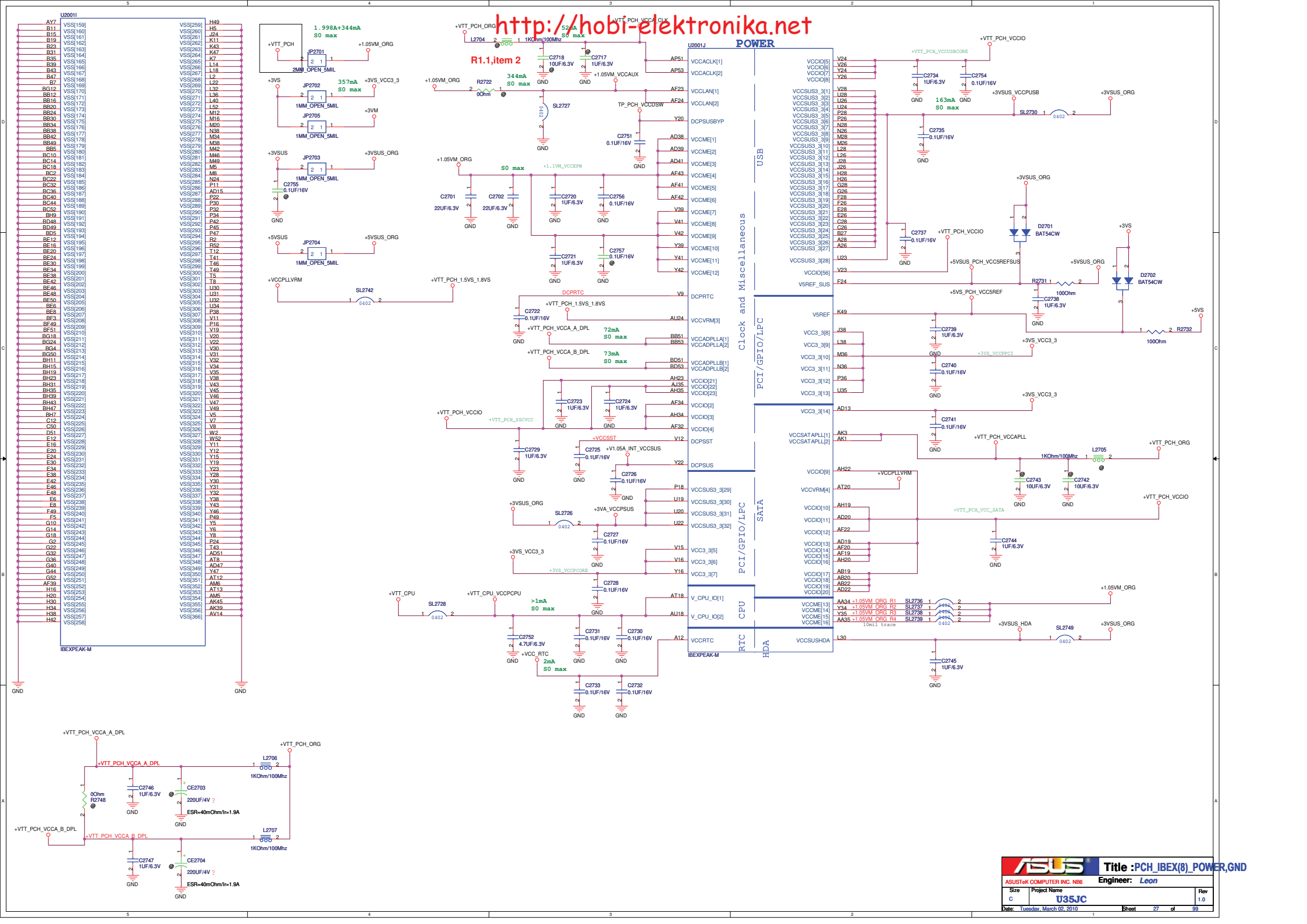
ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(6)CPU,GPIO,MISC
	Engineer: Leon
Size: C	Project Name: U35JC
	Rev: 1.0
Date: Friday, April 09, 2010	Sheet 25 of 99

http://hobi-elektronika.net



ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(7)_POWER,GND
	Engineer: Leon
Size: C	Project Name: U35JC
Rev: 1.0	
Date: Friday, April 09, 2010	Sheet 26 of 99

http://hobi-elektronika.net



ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(8)_POWER,GND
Engineer: Leon	
Size: C	Project Name: U35JC
Rev: 1.0	
Date: Tuesday, March 02, 2010	Sheet 27 of 99

PCH SPI ROM

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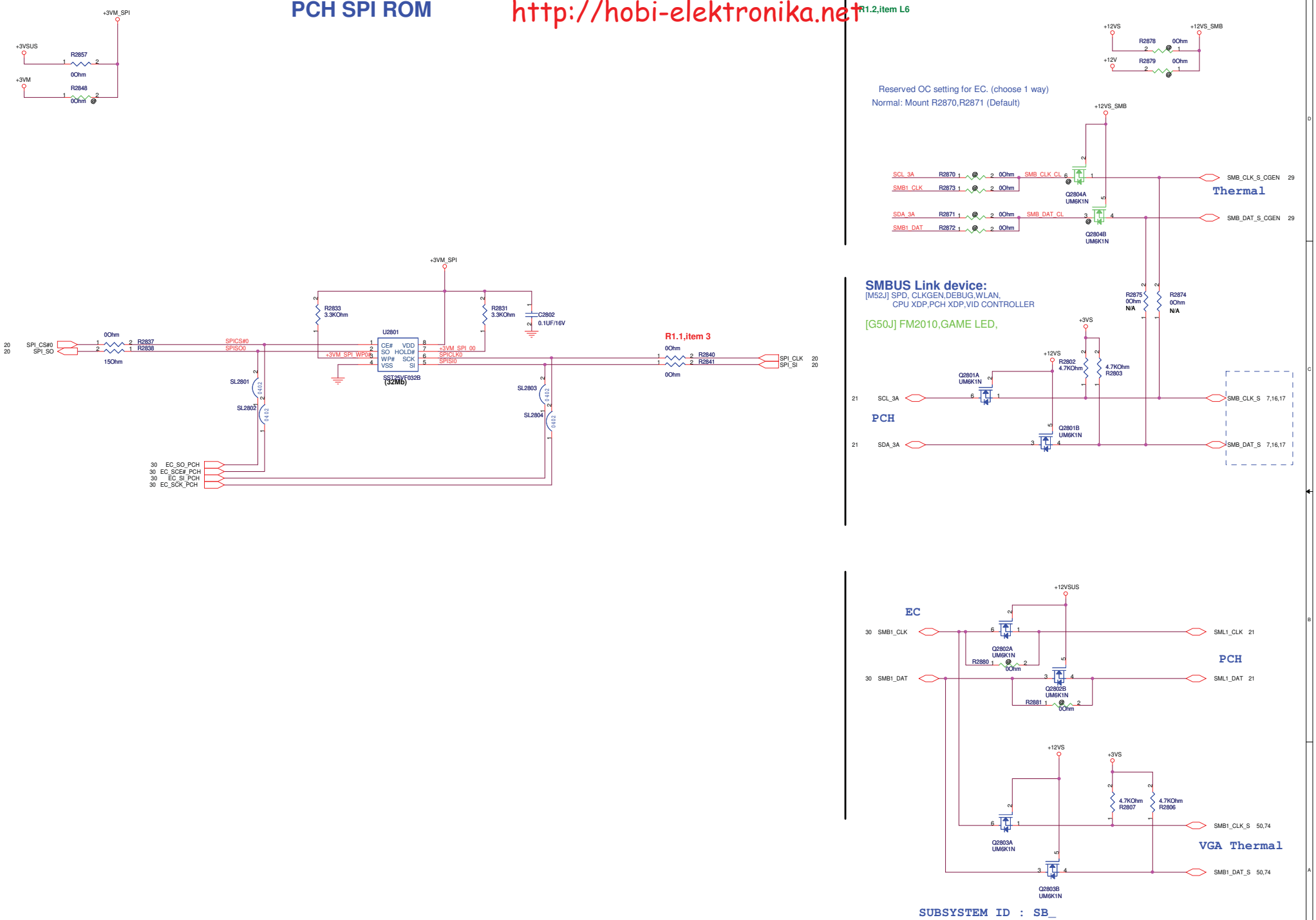
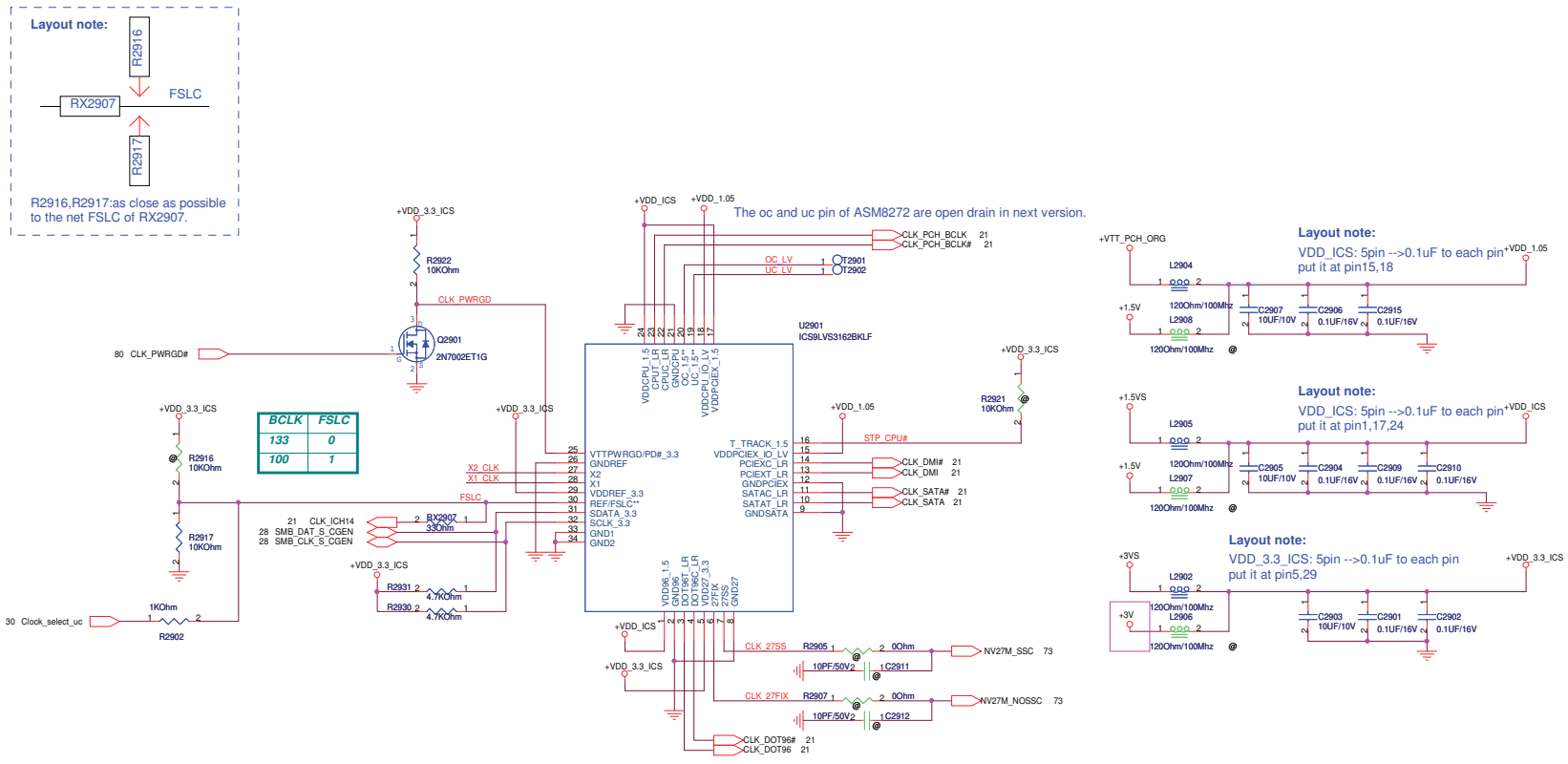


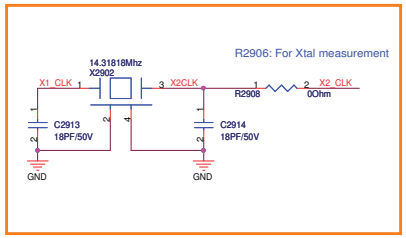
SUBSYSTEM ID : ROM

ASUSTeK COMPUTER INC. NB6	Title : PCH_SPI ROM,OTH	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
Date: Friday, April 09, 2010	Sheet 28 of 99	

http://hobi-elektronika.net

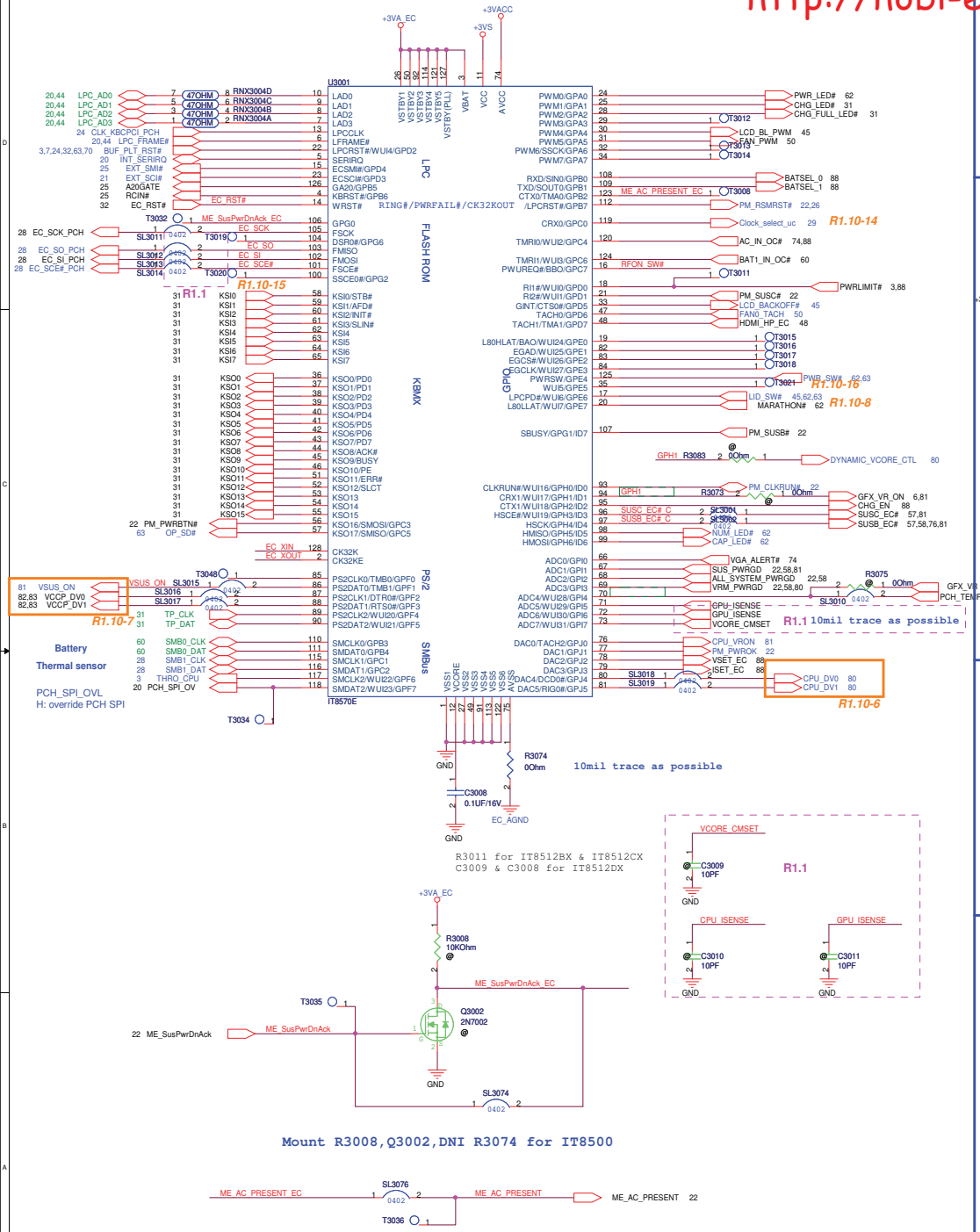


BCLK	FSLC
133	0
100	1

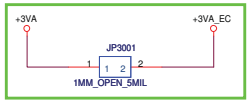


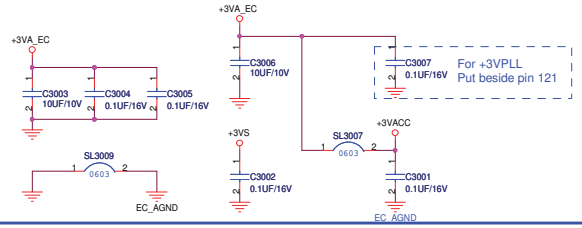
ASUSTeK COMPUTER INC.	Title : CLK_ICS9LRS3197		
	Engineer: Leon		
Size C	Project Name U35JC		Rev 1.0
Date: Friday, April 09, 2010		Sheet 29 of 99	

http://hobi-elektronika.net

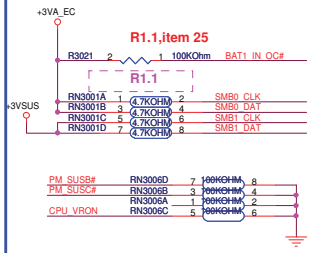


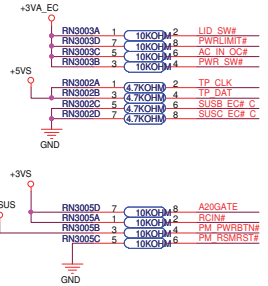
For IT8541 Power





For PU / PD

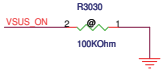




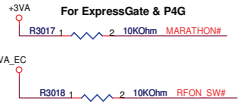
For Instant Key

Note: Close to EC

R1.1,item 6



For ExpressGate & P4G

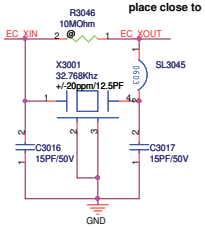


iAMT EC strapping need to check

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.

For X'tal

Note:
Cload=12.5PF place close to EC



For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

R3045: For Xtal measurement

For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

ASUS / ASUSTeK COMPUTER INC.	Title : EC_IT8570		
	Engineer: Leon		
Size: C	Project Name: U35JC		Rev: 1.0
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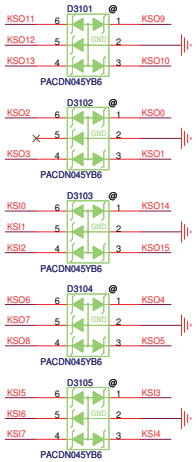
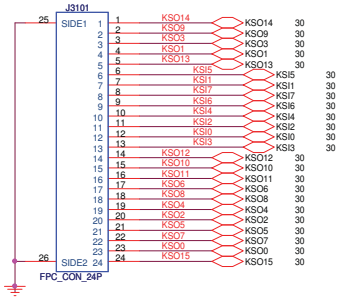


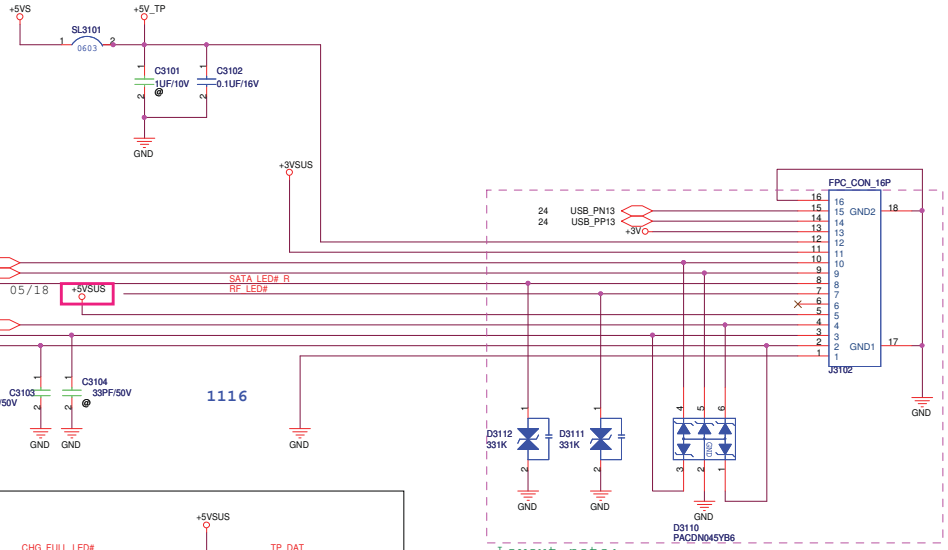
Keyboard



Layout note:
For U33JT ESD,place near J3103

Touch-Pad Conn.

UL30JT,UL33JT colay for ME request.



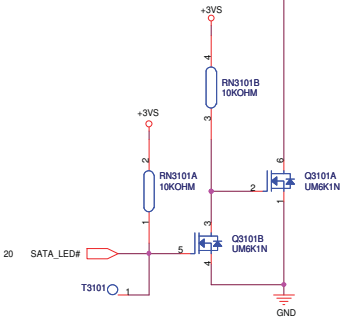
Layout note:
For UL30JT ESD,place near J3102

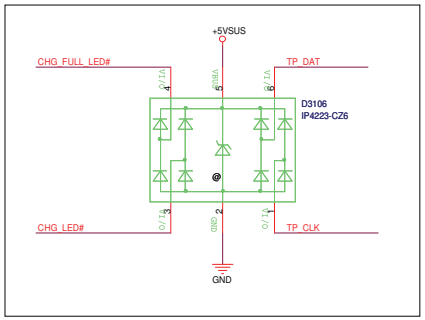
IF=5mA
VF Min. 2.55V
VF Max. 3.25V
ICH9 Sink
Current Max
6mA

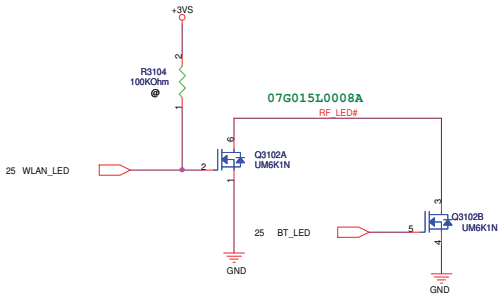
WireLess/BT LED

IF=5mA
VF Min. 2.55V
VF Max. 3.25V

南橋只能sink 6mA







WirelessLAN & Bluetooth Status LED

ASUSTeK COMPUTER INC. NB4	Title : EC_KB, TP	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
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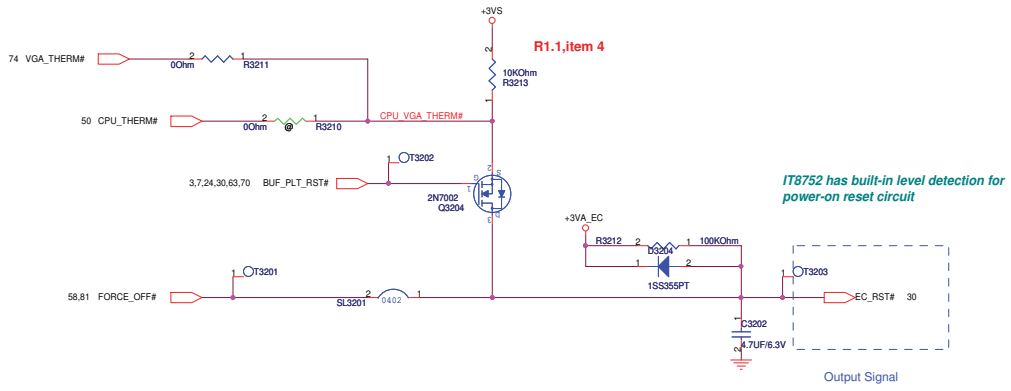
Thermal Policy



ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: Leon	
Size C	Project Name U35JC	Rev 1.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
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<Variant Name>

ASUSTeK COMPUTER INC.

Title : <Title>

Engineer: Leon

Size	Project Name	Rev
C	U35JC	1.0

Date: Tuesday, March 02, 2010 Sheet 34 of 99

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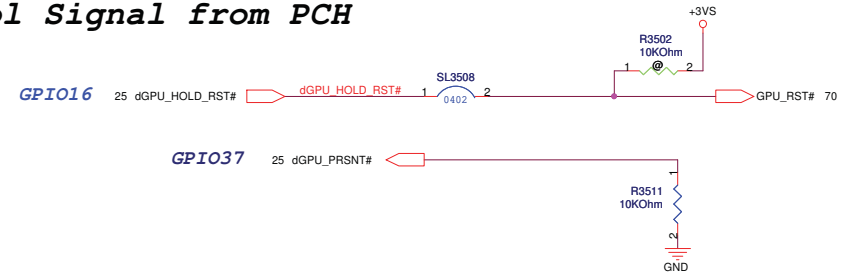
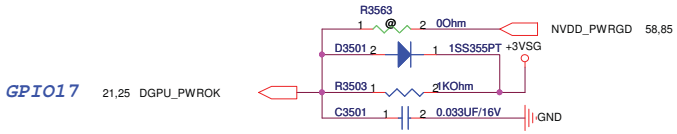
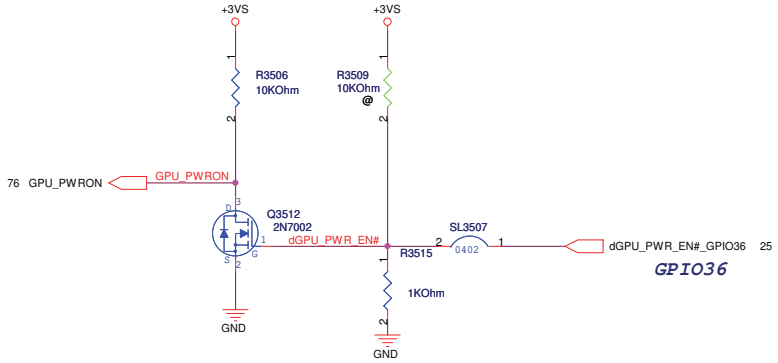
Control Signal from PCH







ASUSTeK COMPUTER INC. NB1	Title : Hybrid Switch		
	Engineer: Leon		
Size: Custom	Project Name: U35JC		Rev: 1.0
Date: Friday, April 09, 2010	Sheet 35 of 99		

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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
Date: Tuesday, March 02, 2010	Sheet 38 of 99	

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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
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<Variant Name>

ASUSTeK COMPUTER INC.	Title :	Engineer: Leon
Size: C	Project Name: U35JC	Rev: 1.0
Date: Tuesday, March 02, 2010	Sheet 40 of 99	

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<Variant Name>

ASUSTeK COMPUTER INC.	Title :	Engineer: Leon
Size: C	Project Name: U35JC	Rev: 1.0
Date: Tuesday, March 02, 2010	Sheet 41 of 99	

http://hobi-elektronika.net

<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
Date: Tuesday, March 02, 2010	Sheet 42 of 99	

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<Variant Name>

ASUSTeK COMPUTER INC.	Title : <Title>	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
Date: Tuesday, March 02, 2010	Sheet 43 of 99	

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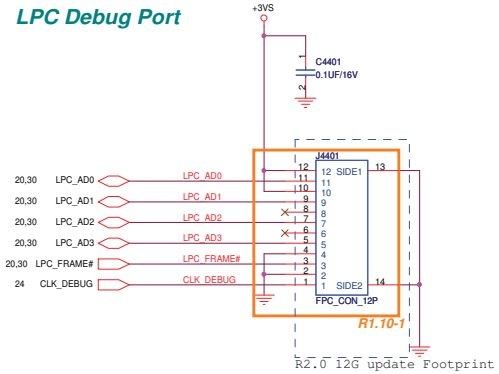
LPC Debug Port



ASUSTeK COMPUTER INC. NB4	Title : BUG_Debug	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
Date: Friday, April 09, 2010	Sheet 44 of 99	

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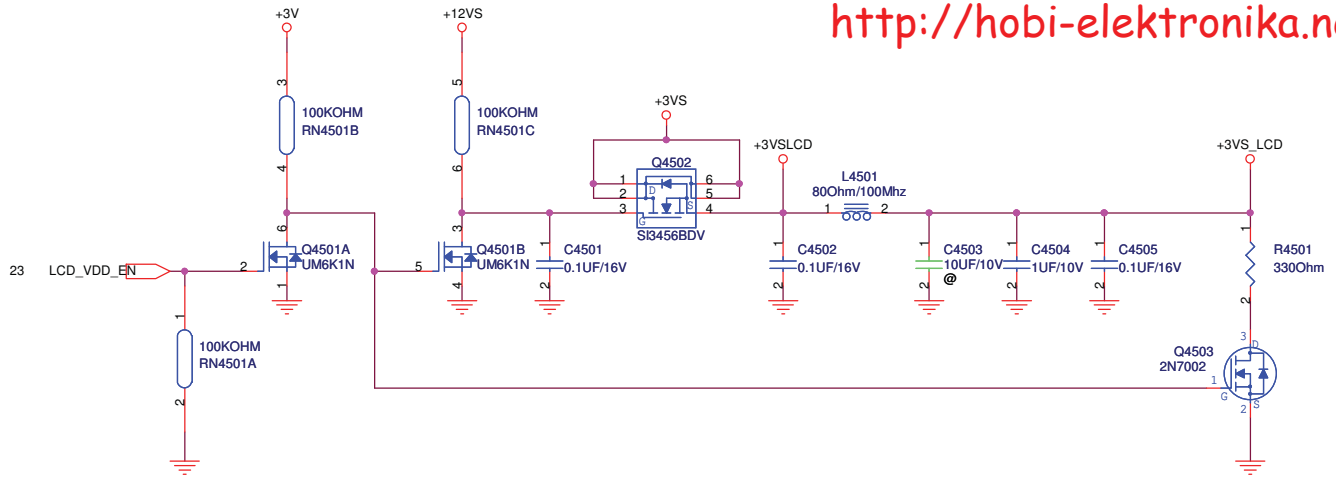
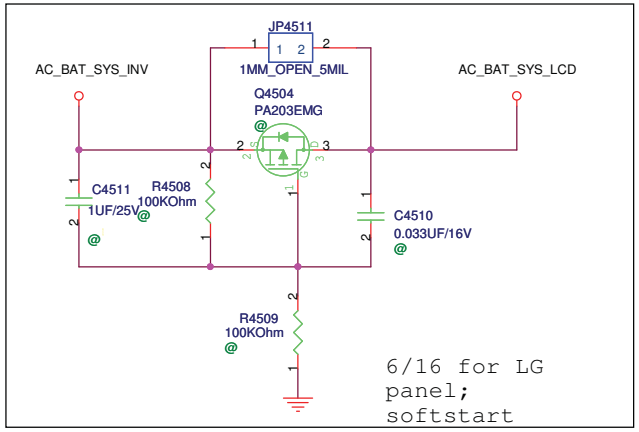
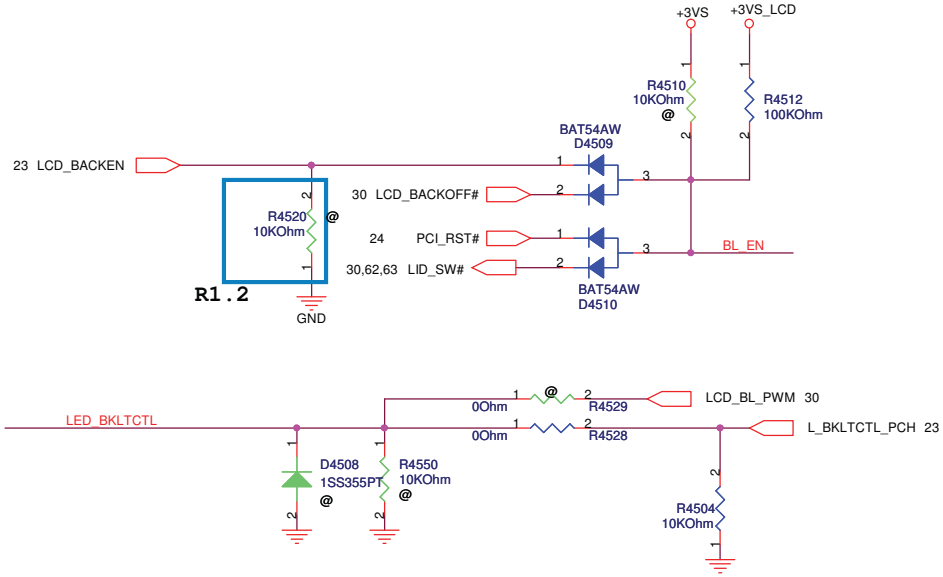
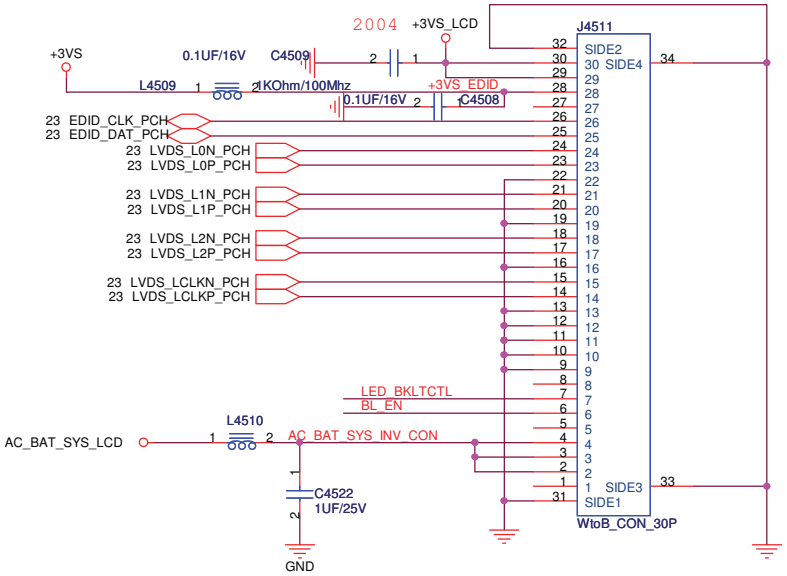
Main Board





LVDS CONN





ASUS	Title : CRT_LCD Panel	
ASUSTeK COMPUTER INC. NB4	Engineer: Leon	
Size B	Project Name U35JC	Rev 1.0
Date: Friday, April 09, 2010	Sheet 45 of 99	

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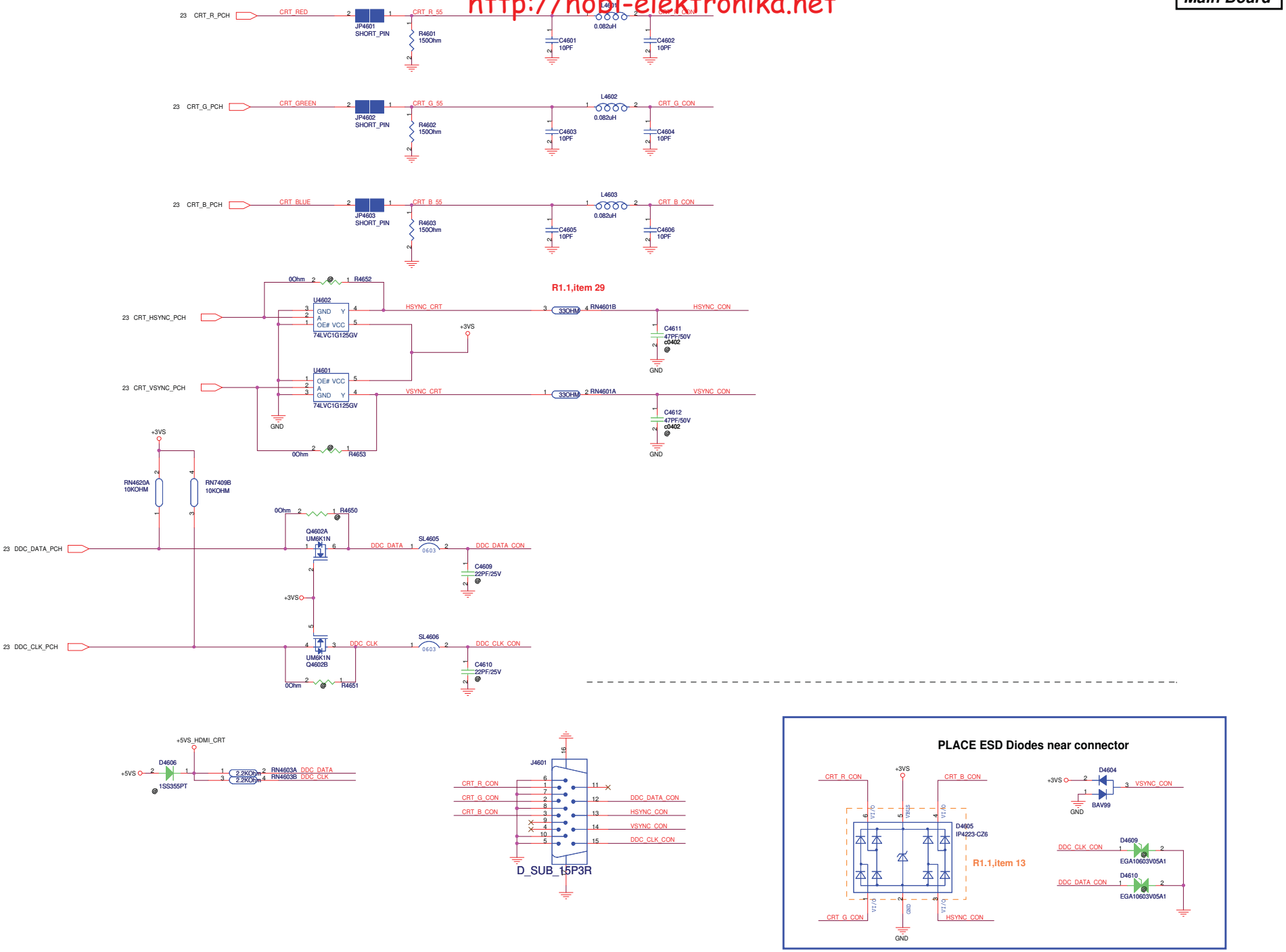
Main Board



ASUSTeK COMPUTER INC. NB4	Title : CRT_D-Sub		
	Engineer: Leon		
Size C	Project Name U35JC		Rev 1.0
Date: Friday, April 09, 2010	Sheet 46 of 99		

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Main Board

ASUSTeK COMPUTER INC. NB4	Title : Display Port	
	Engineer: Leon	
Size C	Project Name U35JC	Rev 1.0
Date: Tuesday, March 02, 2010	Sheet 47 of 99	

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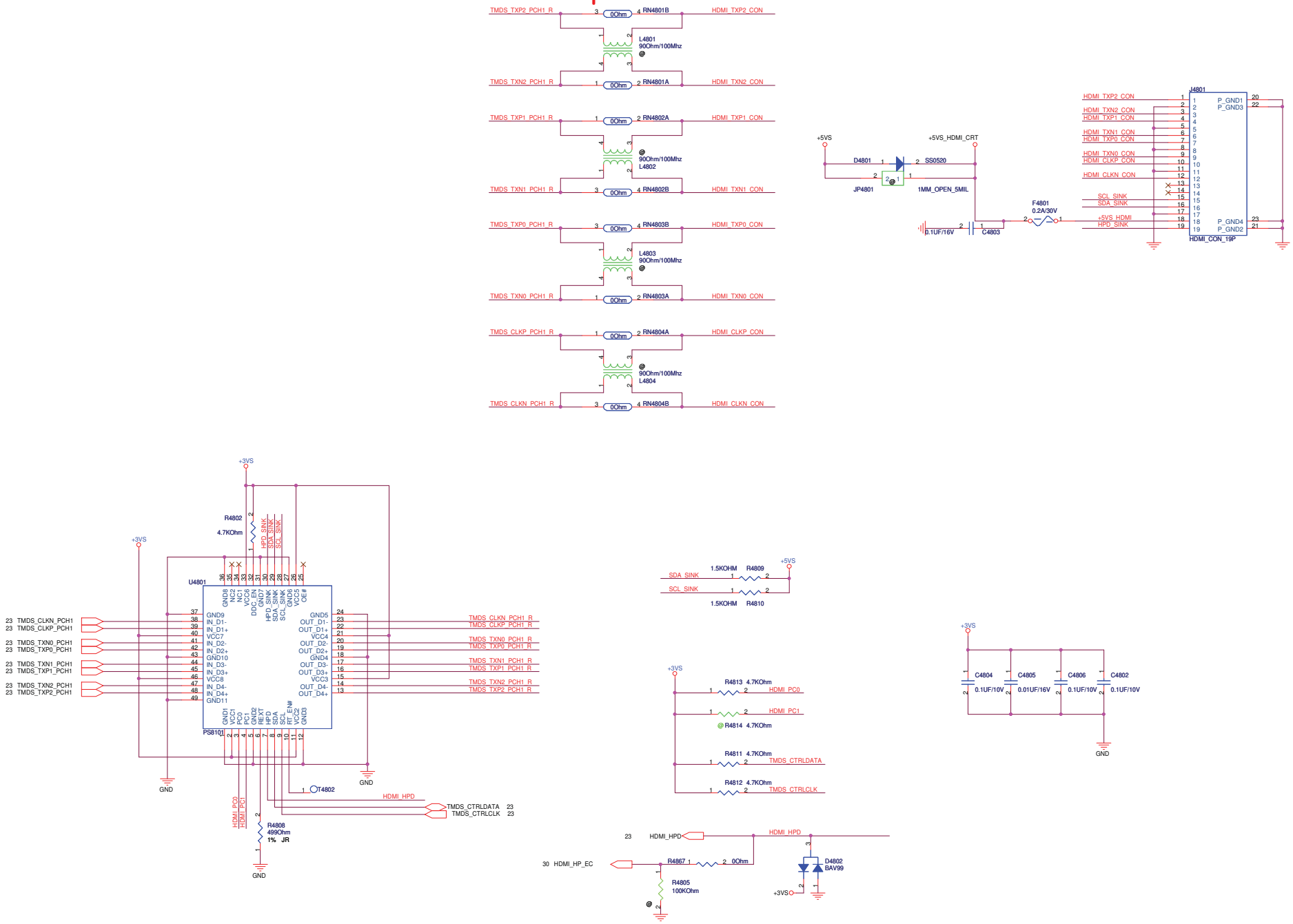

ASUSTeK COMPUTER INC. NB4	Title : TV_HDMI	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
Date: Friday, April 09, 2010	Sheet 46 of 99	

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Main Board

ASUSTeK COMPUTER INC. NB4	Title : TV_****	
	Engineer: Leon	
Size C	Project Name U35JC	Rev 1.0
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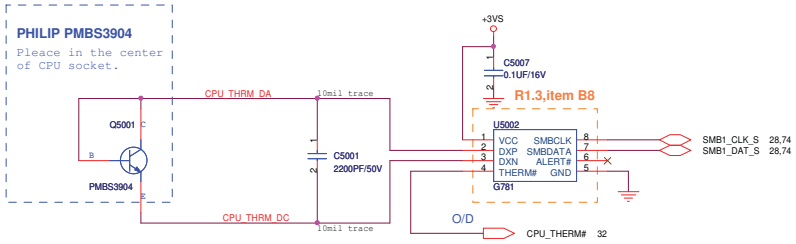
CPU Thermal Sensor

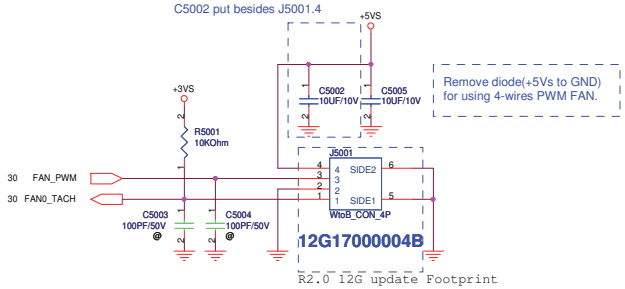


SMBUS addr=1001100x (98)

U5002: Remote(Local) thermal sensor,use remote mode.

R1.10-10

PWM Fan



ASUSTeK COMPUTER INC. NB4	Title : FAN_Fan & Sensor	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
Date: Friday, April 09, 2010	Sheet 50 of 99	

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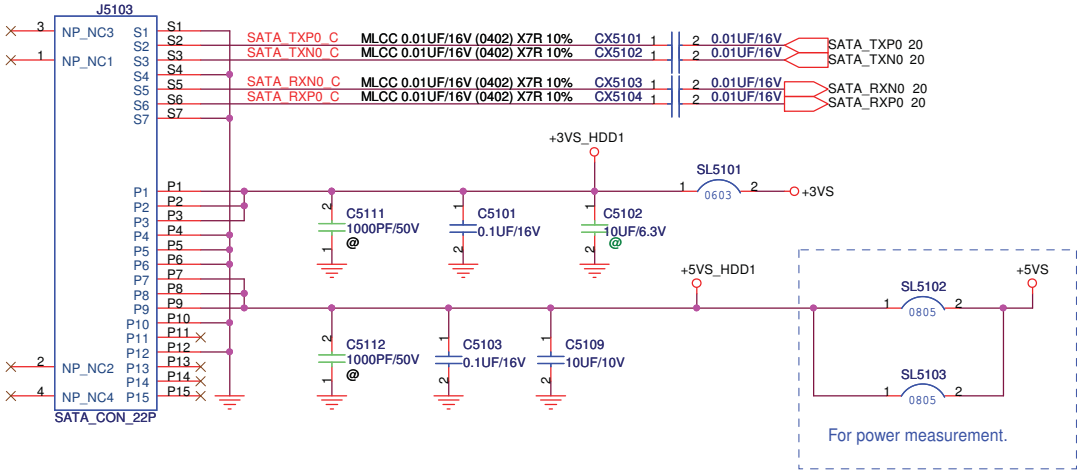
HDD (1st)



ASUSTeK COMPUTER INC. NB4	Title : XDD_HDD	
	Engineer: Leon	
Size B	Project Name U35JC	Rev 1.0
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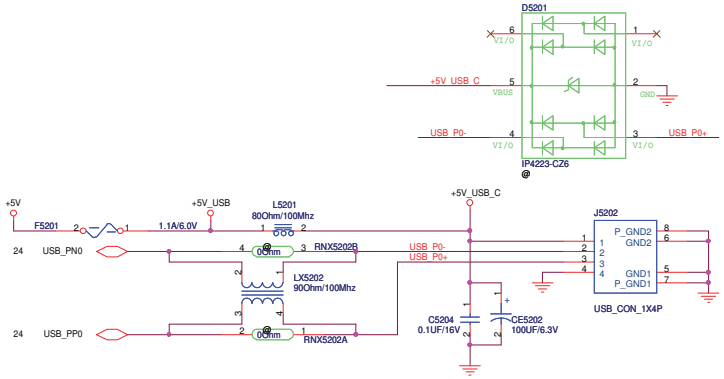
USB ports



ASUSTeK COMPUTER INC. NB4	Title : USB_USB Port *1	Engineer: Leon
Size C	Project Name U35JC	Rev 1.0
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ASUSTeK COMPUTER INC. NB6	Title : MINICARD(WLAN)	Engineer: Leon
Size: C	Project Name: U35JC	Rev: 1.0
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Main Board

ASUSTeK COMPUTER INC. NB4	Title : BAR_****	
	Engineer: Leon	
Size C	Project Name U35JC	Rev 1.0
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Main Board

ASUSTeK COMPUTER INC. NB4	Title : SIO_****	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
Date: Tuesday, March 02, 2010	Sheet 55 of 99	

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Main Board

ASUSTeK COMPUTER INC. NB4	Title : LED_Indicator		
	Engineer: Leon		
Size C	Project Name U35JC		Rev 1.0
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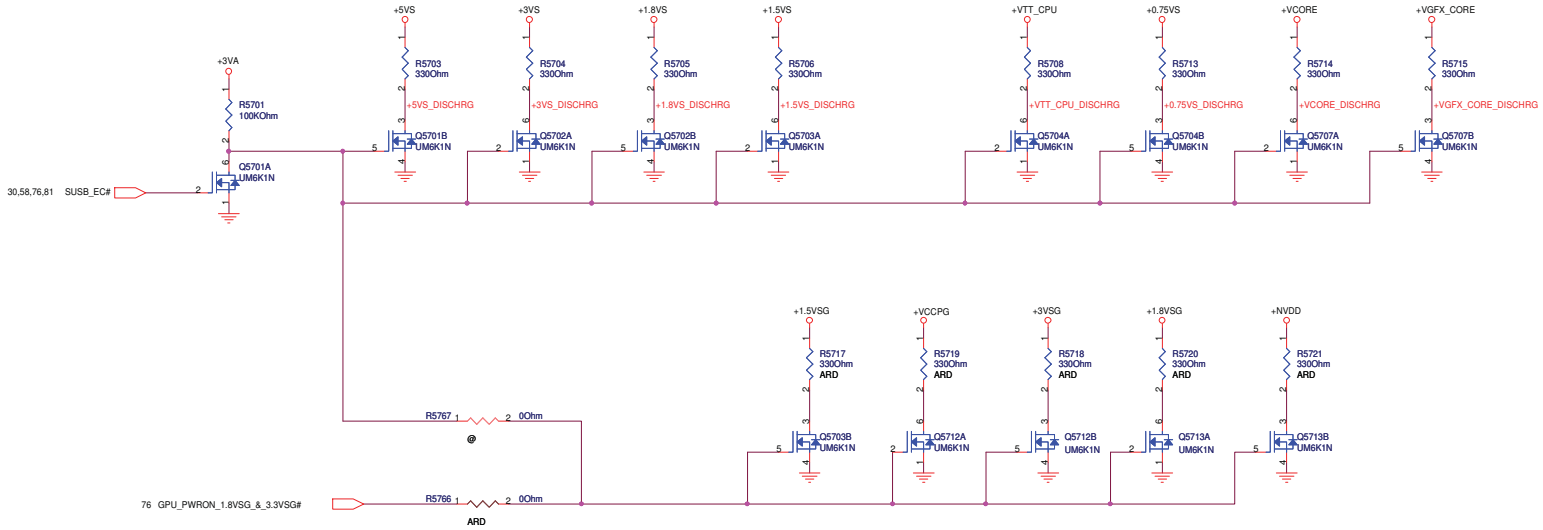
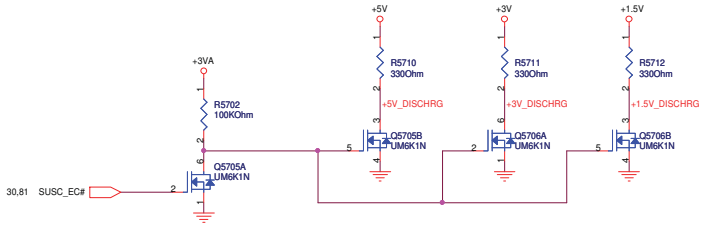
Main Board





ASUSTeK COMPUTER INC. NB4	Title : DSG_Discharge	
	Engineer: Leon	
Size C	Project Name U35JC	Rev 1.0
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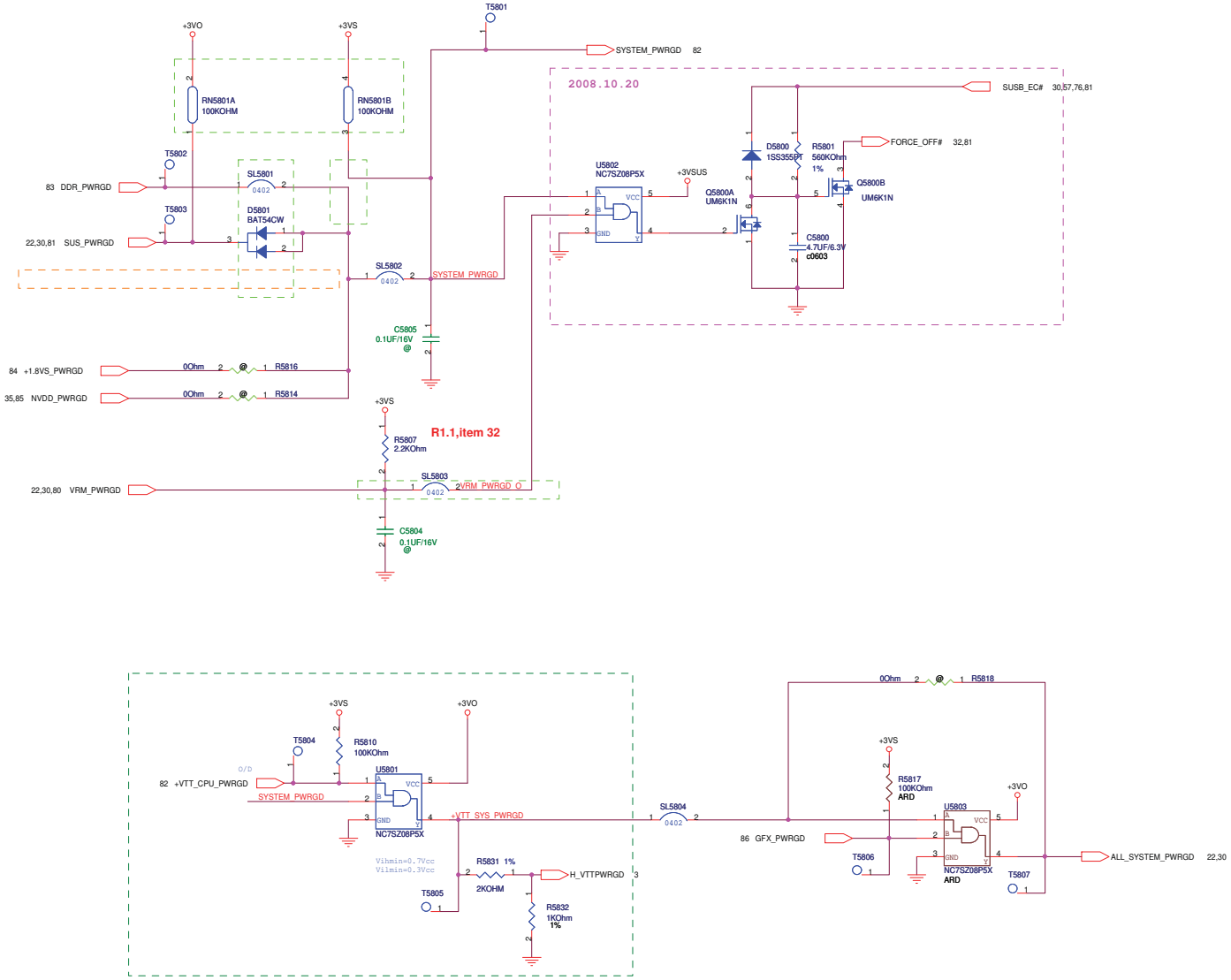
POWER GOOD DETECTER



2008-08-04,James Wu add.

ASUSTeK COMPUTER INC. NB3	Title : POWER_PROTECT	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
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Main Board

ASUSTeK COMPUTER INC. NB4	Title : DJ_****	
	Engineer: Leon	
Size C	Project Name U35JC	Rev 1.0
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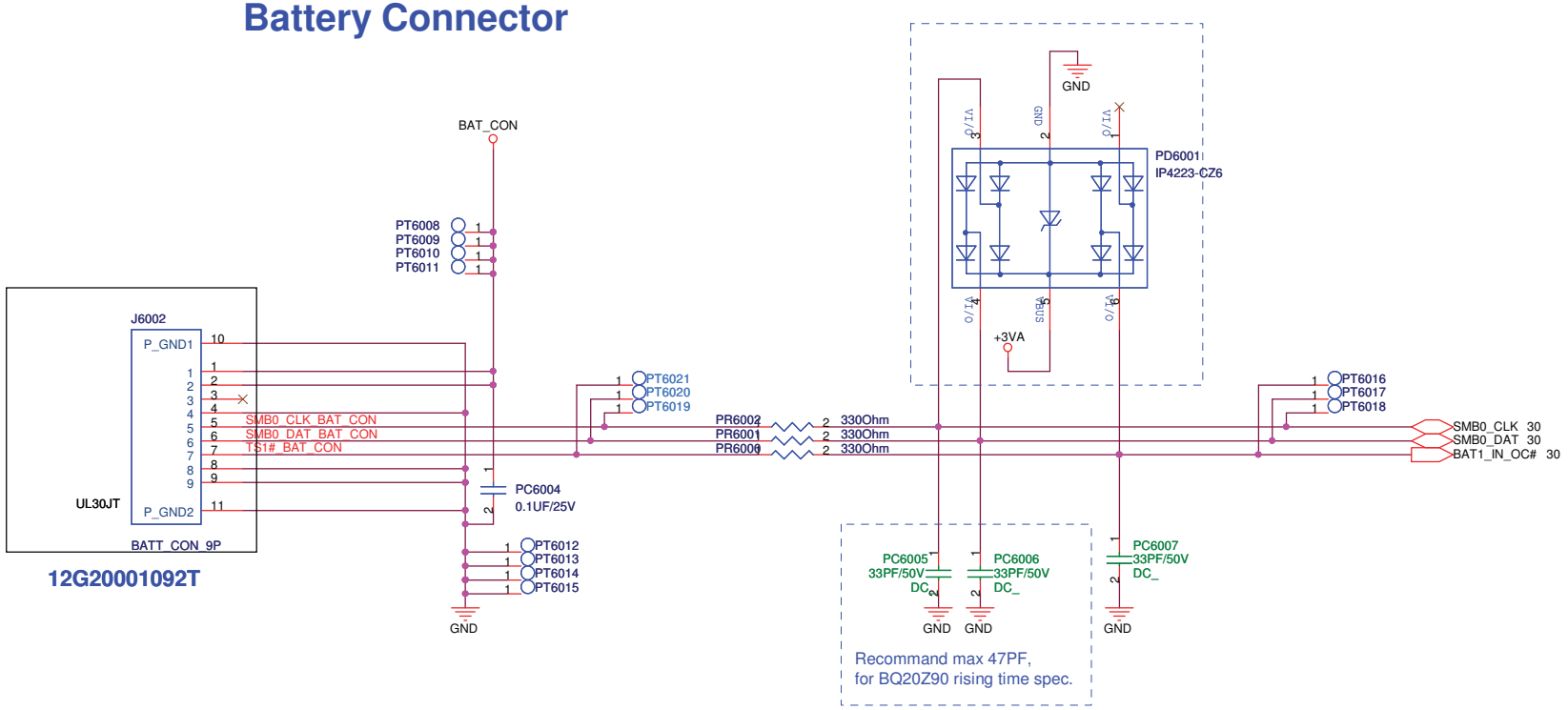
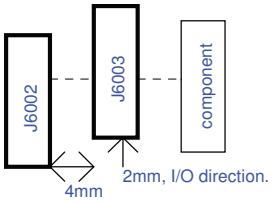
Battery Connector



12G20001092T

```
081111 -> 090604:
1. Change D6005 from DF5A6.8FU to IP4223-CZ6 for cost down and integration.
```

Layout note:
Battery connector colay for UL30JT & U33JT.



ASUS	Title : DC_BAT Conn.	
ASUSTeK COMPUTER INC. NB4	Engineer: Leon	
Size B	Project Name U35JC	Rev 1.0
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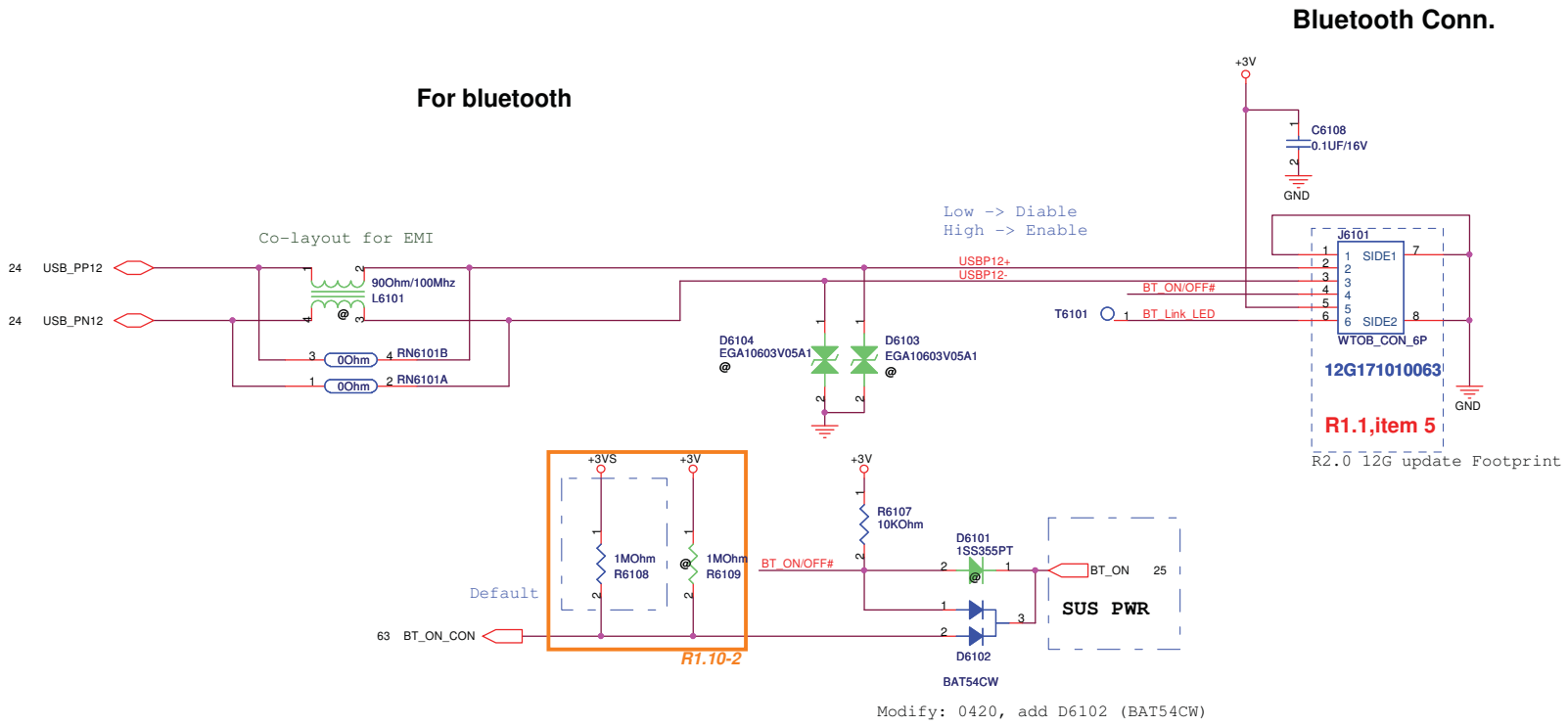

ASUSTeK COMPUTER INC. NB1	Title : BT	Engineer: Leon
Size: Custom	Project Name: U35JC	Rev: 1.0
Date: Friday, April 09, 2010	Sheet 61 of 99	

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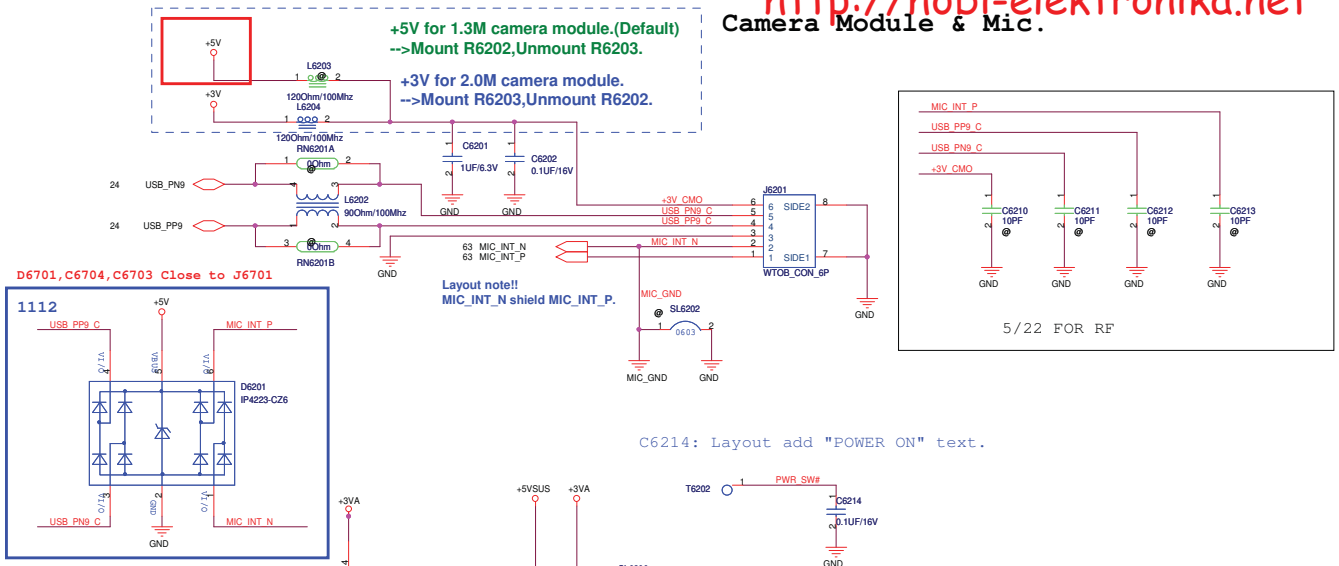
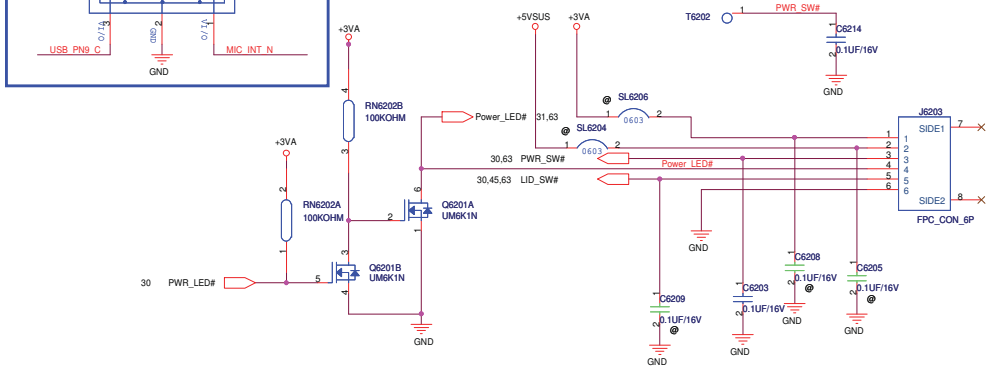
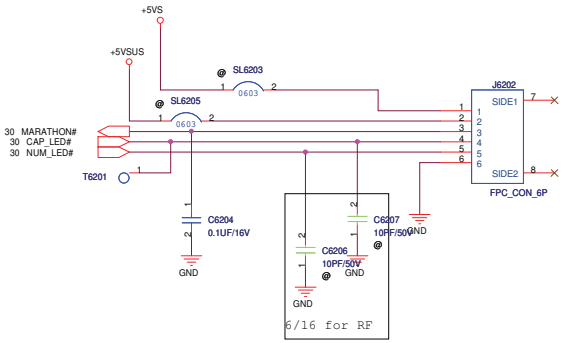
Camera Module & Mic.



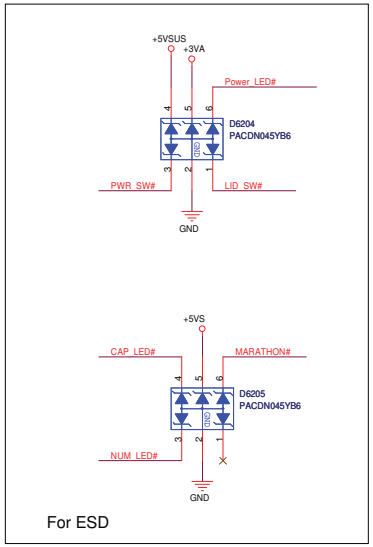
C6214: Layout add "POWER ON" text.



PWR S/W Board



Express gate S/W Board



ASUSTeK COMPUTER INC. NB4	Title : CMO CMOS CAMERA	
	Engineer: Leon	
Size C	Project Name U35JC	Rev 1.0
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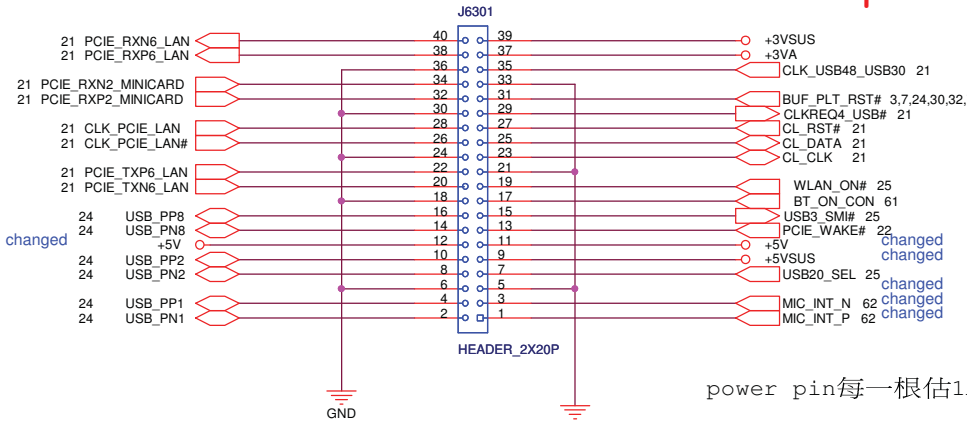
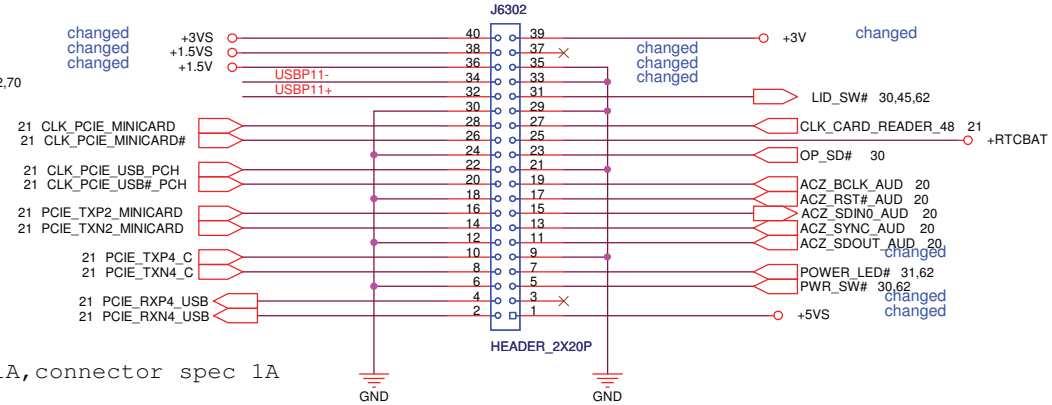
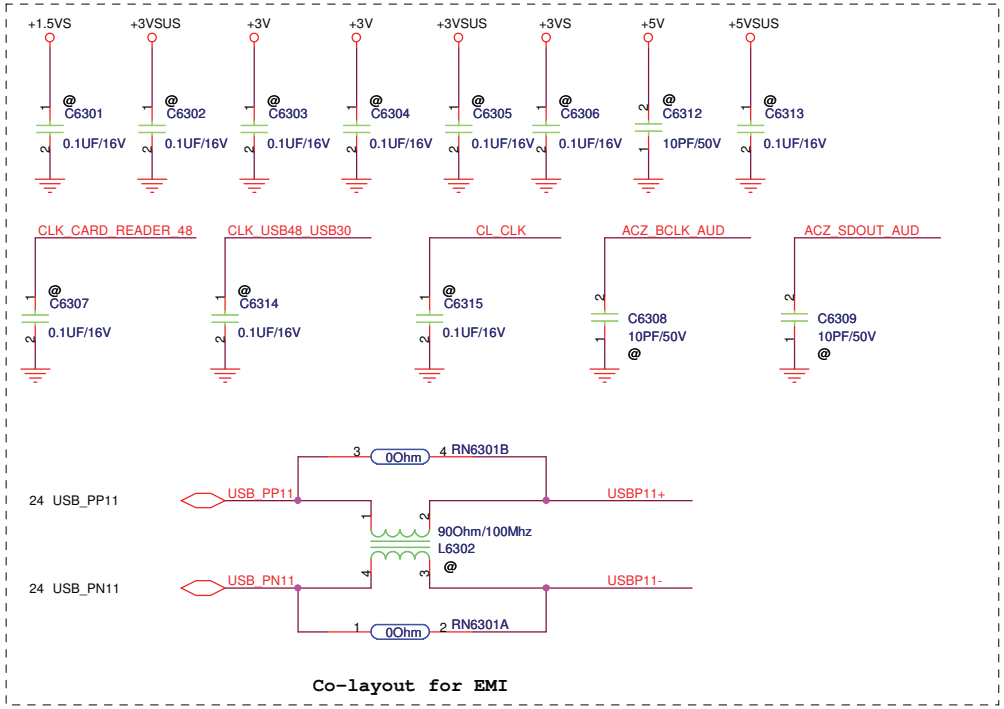
Main Board





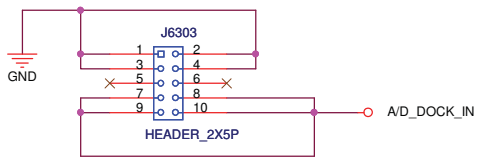
power pin每一根估1A,connector spec 1A

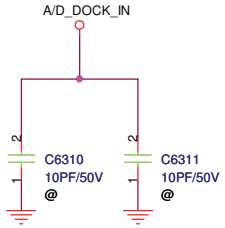
For EMI close to connector



Co-layout for EMI

A/D commector





ASUS	Title : B TO B CONN	
ASUSTeK COMPUTER INC. NB4	Engineer: Leon	
Size B	Project Name U35JC	Rev 1.0
Date: Friday, April 09, 2010	Sheet 63 of 99	

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ASUSTeK COMPUTER INC. NB4	Title : TUN_TV Tuner	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
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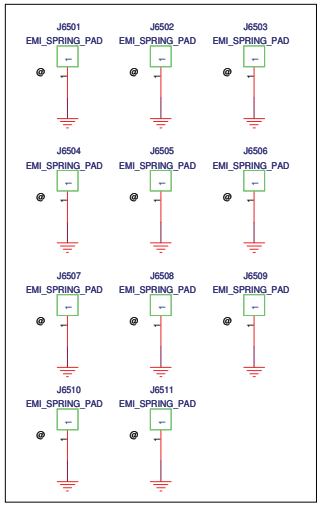
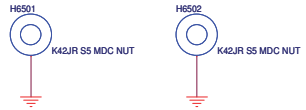
EMI spring for U33JT

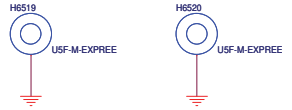


Screw Hole & SMT Nut

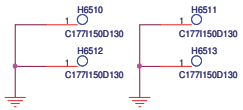
FAN NUT



GPU

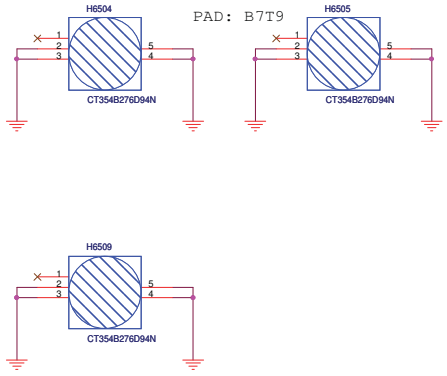


CPU

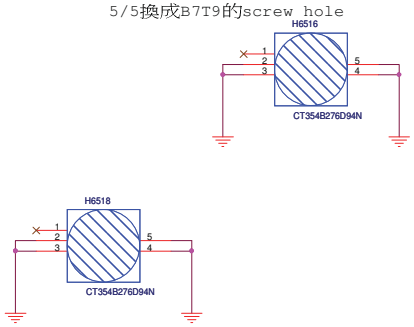


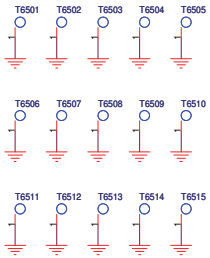
固定孔

PAD: B7T9

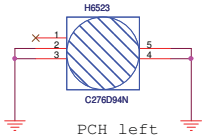


5/5換成B7T9的screw hole



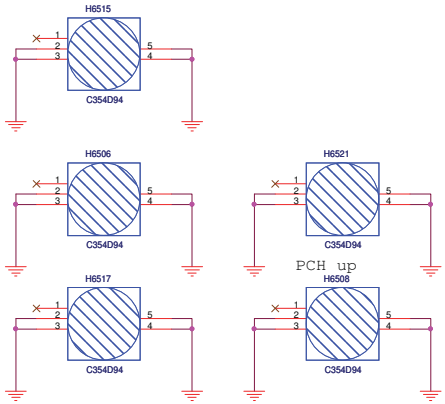


PAD: B7T7

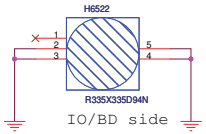


PCH left

PAD: B9T9



PCH up



IO/BD side

ASUSTeK COMPUTER INC. NB4	Title : ME_Conn & Skew Hole	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
Date: Wednesday, April 07, 2010	Sheet 65 of 99	

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Main Board

ASUSTeK COMPUTER INC. NB4	Title : ESA_ESATA	
	Engineer: Leon	
Size C	Project Name U35JC	Rev 1.0
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ASUSTeK COMPUTER INC. NB4	Title : PCH_XDP, ONFI	
Size: C	Project Name: U35JC	Rev: 1.0
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Title <Title>		
Size A	Document Number U35JC	Rev 1.0
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0.3B Beta

ASUSTeK COMPUTER INC. NB4	Title : USB 3.0_NEC (2)	
	Engineer: Leon	
Size A3	Project Name U35JC	Rev 1.0
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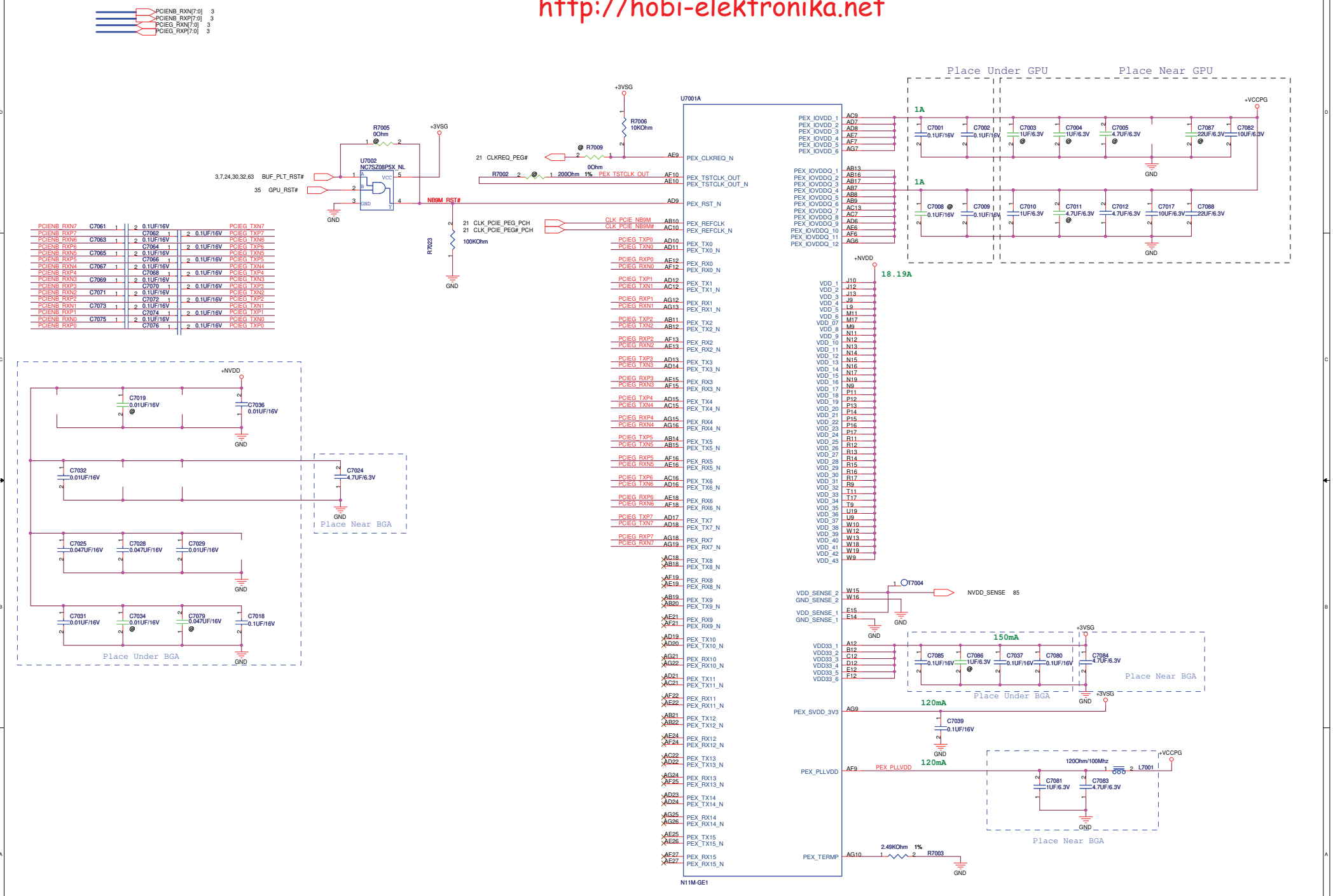

PCIENB_RXN7	C7061	0.1UF/16V	C7062	0.1UF/16V	PCIEG_TXN7
PCIENB_RXP7					PCIEG_TXP7
PCIENB_RXN6	C7063	0.1UF/16V	C7064	0.1UF/16V	PCIEG_TXN6
PCIENB_RXP6					PCIEG_TXP6
PCIENB_RXN5	C7065	0.1UF/16V	C7066	0.1UF/16V	PCIEG_TXN5
PCIENB_RXP5					PCIEG_TXP5
PCIENB_RXN4	C7067	0.1UF/16V	C7068	0.1UF/16V	PCIEG_TXN4
PCIENB_RXP4					PCIEG_TXP4
PCIENB_RXN3	C7069	0.1UF/16V	C7070	0.1UF/16V	PCIEG_TXN3
PCIENB_RXP3					PCIEG_TXP3
PCIENB_RXN2	C7071	0.1UF/16V	C7072	0.1UF/16V	PCIEG_TXN2
PCIENB_RXP2					PCIEG_TXP2
PCIENB_RXN1	C7073	0.1UF/16V	C7074	0.1UF/16V	PCIEG_TXN1
PCIENB_RXP1					PCIEG_TXP1
PCIENB_RXN0	C7075	0.1UF/16V	C7076	0.1UF/16V	PCIEG_TXN0
PCIENB_RXP0					PCIEG_TXP0

PCIEG_TXP0	AD10	PEX_TX0	PCIEG_RXP4	AG15	PEX_RX4
PCIEG_TXN0	AD11	PEX_TX0_N	PCIEG_RXN4	AG16	PEX_RX4_N
PCIEG_RXP0	AE12	PEX_RX0	PCIEG_TXP5	AB14	PEX_TX5
PCIEG_RXN0	AF12	PEX_RX0_N	PCIEG_TXN5	AB15	PEX_TX5_N
PCIEG_TXP1	AD12	PEX_TX1	PCIEG_RXP5	AF16	PEX_RX5
PCIEG_TXN1	AC12	PEX_TX1_N	PCIEG_RXN5	AE16	PEX_RX5_N
PCIEG_RXP1	AG12	PEX_RX1	PCIEG_TXP6	AC16	PEX_TX6
PCIEG_RXN1	AG13	PEX_RX1_N	PCIEG_TXN6	AD16	PEX_TX6_N
PCIEG_TXP2	AB11	PEX_TX2	PCIEG_RXP6	AE18	PEX_RX6
PCIEG_TXN2	AB12	PEX_TX2_N	PCIEG_RXN6	AF18	PEX_RX6_N
PCIEG_RXP2	AF13	PEX_RX2	PCIEG_TXP7	AD17	PEX_TX7
PCIEG_RXN2	AE13	PEX_RX2_N	PCIEG_TXN7	AD18	PEX_TX7_N
PCIEG_TXP3	AD13	PEX_TX3	PCIEG_RXP7	AG18	PEX_RX7
PCIEG_TXN3	AD14	PEX_TX3_N	PCIEG_RXN7	AG19	PEX_RX7_N
PCIEG_RXP3	AE15	PEX_RX3		AC18	PEX_TX8
PCIEG_RXN3	AF15	PEX_RX3_N		AB18	PEX_TX8_N
PCIEG_TXP4	AD15	PEX_TX4		AF19	PEX_RX8
PCIEG_TXN4	AC15	PEX_TX4_N		AE19	PEX_RX8_N
				AB19	PEX_TX9
				AB20	PEX_TX9_N
				AE21	PEX_RX9
				AF21	PEX_RX9_N
				AD19	PEX_TX10
				AD20	PEX_TX10_N
				AG21	PEX_RX10
				AG22	PEX_RX10_N
				AD21	PEX_TX11
				AC21	PEX_TX11_N
				AF22	PEX_RX11
				AE22	PEX_RX11_N
				AB21	PEX_TX12
				AB22	PEX_TX12_N
				AE24	PEX_RX12
				AF24	PEX_RX12_N
				AC22	PEX_TX13
				AD22	PEX_TX13_N
				AG24	PEX_RX13
				AF25	PEX_RX13_N
				AD23	PEX_TX14
				AD24	PEX_TX14_N
				AG25	PEX_RX14
				AG26	PEX_RX14_N
				AE25	PEX_TX15
				AE26	PEX_TX15_N
				AF27	PEX_RX15
				AE27	PEX_RX15_N

PEX_IOVDD_1	AC9	C7001 0.1UF/16V	C7002 0.1UF/16V	C7003 1UF/6.3V @	C7004 1UF/6.3V @
PEX_IOVDD_2	AD7				
PEX_IOVDD_3	AD8				
PEX_IOVDD_4	AE7				
PEX_IOVDD_5	AF7				
PEX_IOVDD_6	AG7				
PEX_IOVDDQ_1	AB13	C7008 @ 0.1UF/16V	C7009 0.1UF/16V	C7010 1UF/6.3V	C7011 4.7UF/6.3V @
PEX_IOVDDQ_2	AB16				
PEX_IOVDDQ_3	AB17				
PEX_IOVDDQ_4	AB7				
PEX_IOVDDQ_5	AB8				
PEX_IOVDDQ_6	AB9				
PEX_IOVDDQ_7	AC13				
PEX_IOVDDQ_8	AC7				
PEX_IOVDDQ_9	AD6				
PEX_IOVDDQ_10	AE6				
PEX_IOVDDQ_11	AF6				
PEX_IOVDDQ_12	AG6				

C7005 4.7UF/6.3V @	C7087 22UF/6.3V @	C7082 10UF/6.3V	C7012 4.7UF/6.3V	C7017 10UF/6.3V	C7088 22UF/6.3V

VDD_1	J10	VDD_22	P16	VDD_35	U19
VDD_2	J12	VDD_23	P17	VDD_36	U9
VDD_3	J13	VDD_24	R11	VDD_37	W10
VDD_4	J9	VDD_25	R12	VDD_38	W12
VDD_5	L9	VDD_26	R13	VDD_39	W13
VDD_6	M11	VDD_27	R14	VDD_40	W18
VDD_07	M17	VDD_28	R15	VDD_41	W19
VDD_8	M9	VDD_29	R16	VDD_42	W9
VDD_9	N11	VDD_30	R17	VDD_43	
VDD_10	N12	VDD_31	R9		
VDD_11	N13	VDD_32	T11		
VDD_12	N14	VDD_33	T17		
VDD_13	N15	VDD_34	T9		
VDD_14	N16				
VDD_15	N17				
VDD_16	N19				
VDD_17	N9				
VDD_18	P11				
VDD_19	P12				
VDD_20	P13				
VDD_21	P14				
VDD_22	P15				

VDD33_1	A12	C7085 0.1UF/16V	C7086 1UF/6.3V @	C7037 0.1UF/16V	C7080 0.1UF/16V
VDD33_2	B12				
VDD33_3	C12				
VDD33_4	D12				
VDD33_5	E12				
VDD33_6	F12				

C7084 4.7UF/6.3V	C7019 0.01UF/16V @	C7036 0.01UF/16V	C7032 0.01UF/16V	C7024 4.7UF/6.3V	C7025 0.047UF/16V
C7028 0.047UF/16V	C7029 0.01UF/16V	C7031 0.01UF/16V	C7034 0.01UF/16V @	C7079 0.047UF/16V @	C7018 0.1UF/16V
C7039 0.1UF/16V	C7081 1UF/6.3V	C7083 4.7UF/6.3V			

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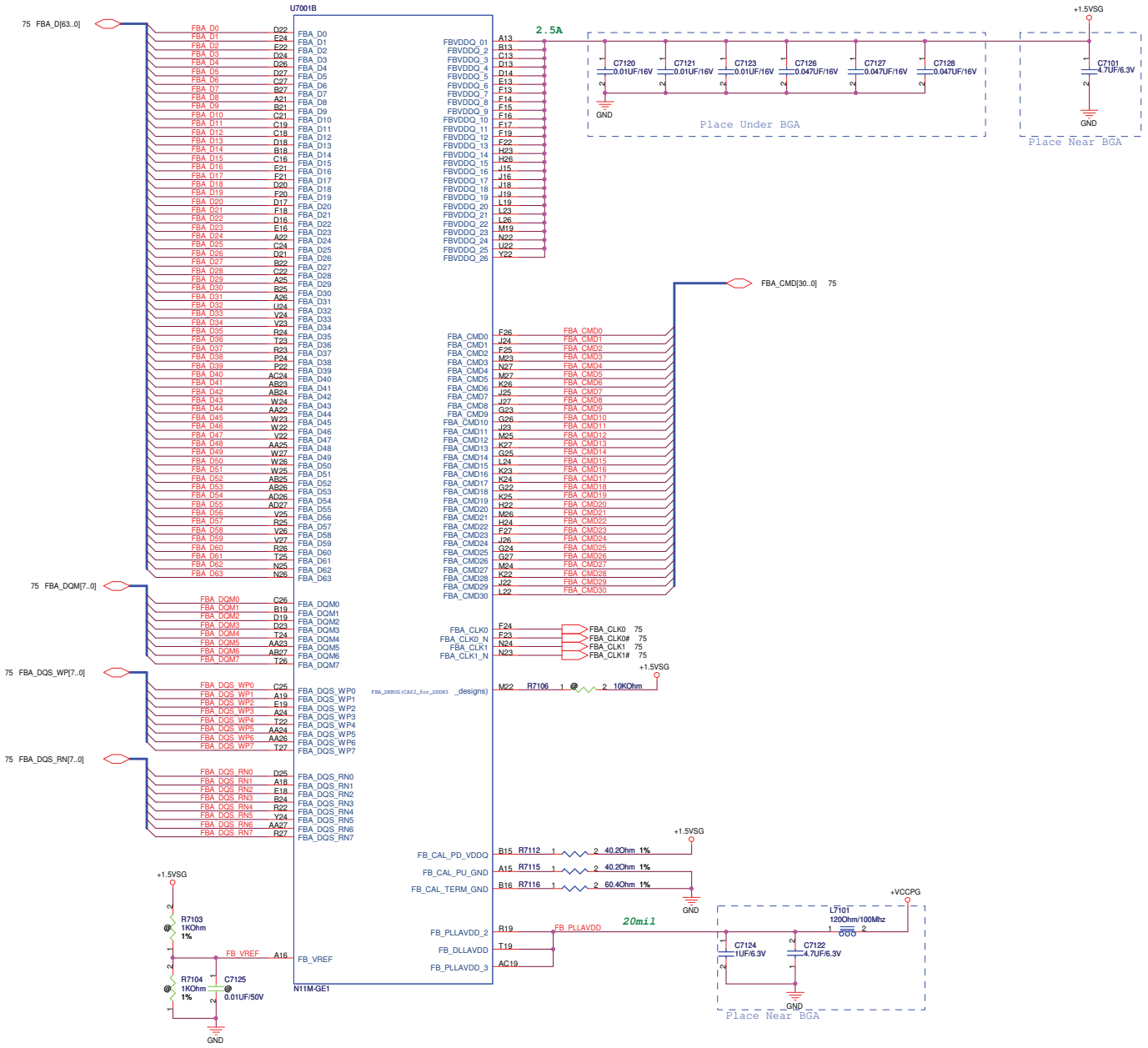

ASUSTeK COMPUTER INC.	Title : N10M-GE1 (2)		
	Engineer: Leon		
Size C	Project Name U35JC		Rev 1.0
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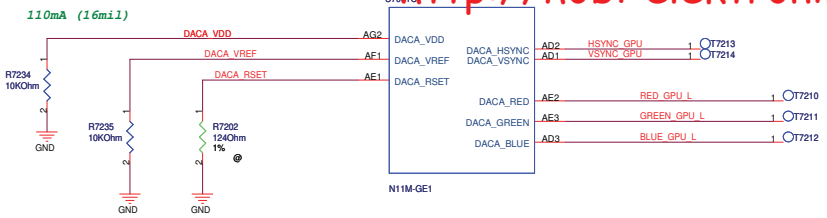
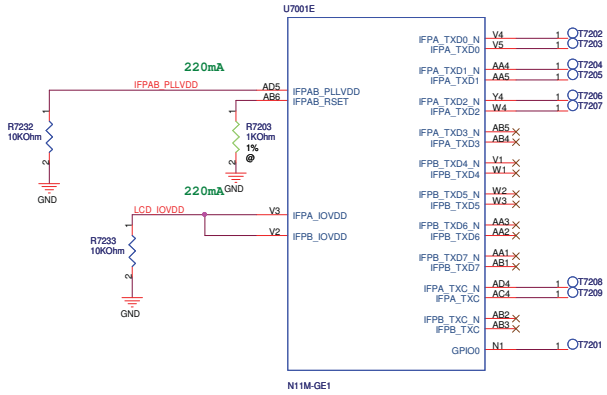
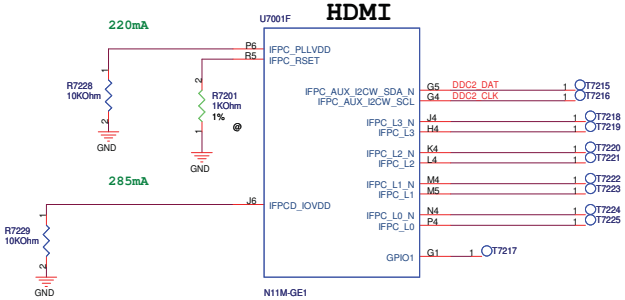
VGA



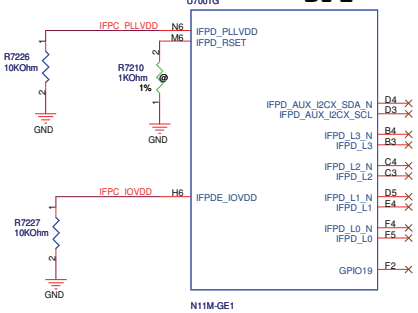
LVDS

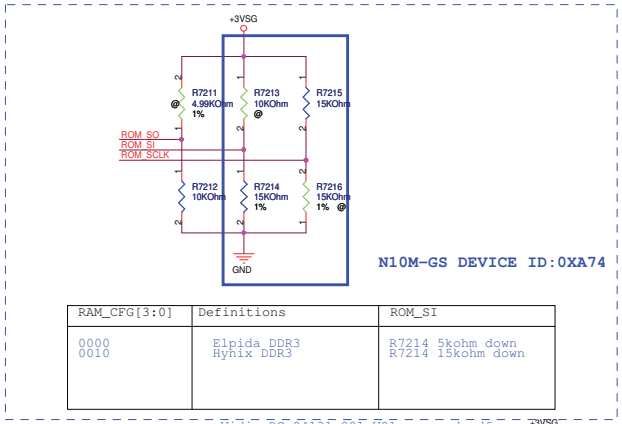


HDMI



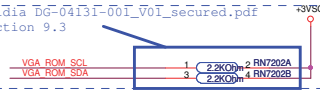
DP1





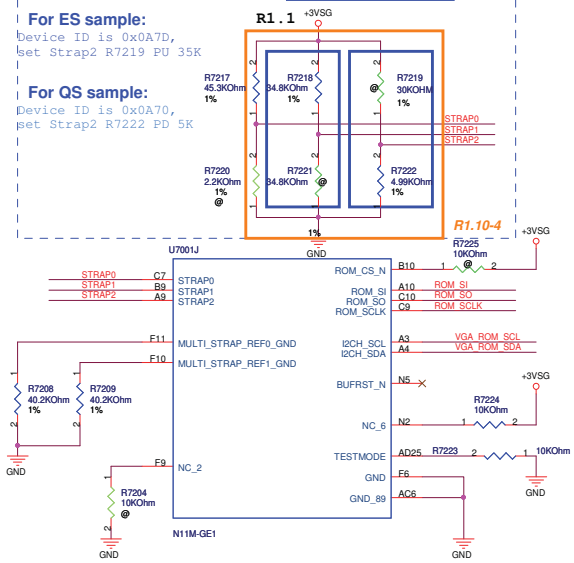
RAM_CFG[3:0]	Definitions	ROM_SI
0000 0010	Elpida DDR3 Hynix DDR3	R7214 5kohm down R7214 15kohm down

nVidia DG-04131-001_V01_secured.pdf
section 9.3



For ES sample:
Device ID is 0x0A7D,
set Strap2 R7219 PU 35K

For QS sample:
Device ID is 0x0A70,
set Strap2 R7222 PD 5K



ASUSTeK COMPUTER INC. (Valiant Series)	Title : N10M-GE1 (3)	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
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Xtal

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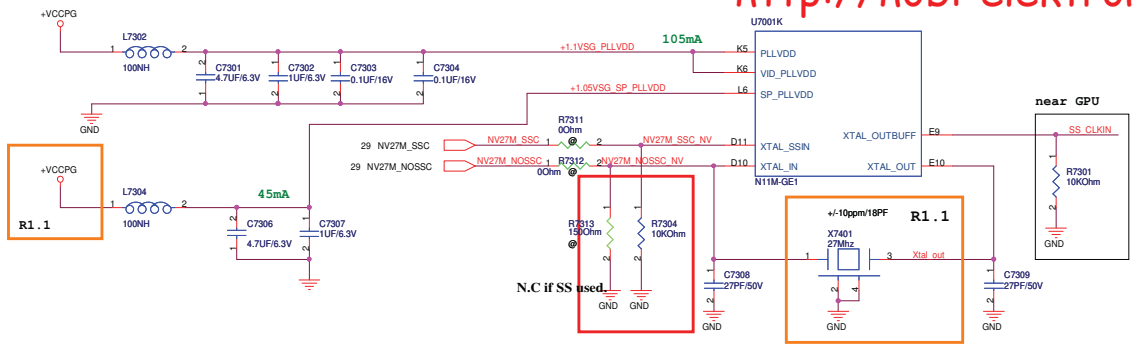
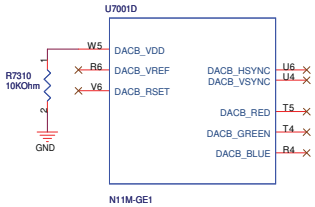
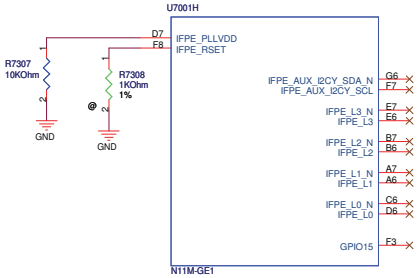
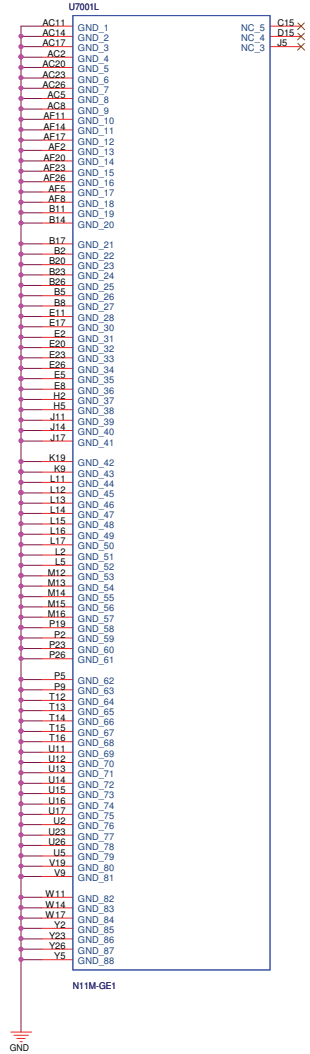


Other







ASUSTeK COMPUTER INC.	Title : N10M-GE1 (4)	
	Engineer: Leon	
Size: C	Project Name: U35JC	Rev: 1.0
Date: Friday, April 09, 2010	Sheet 73 of 99	

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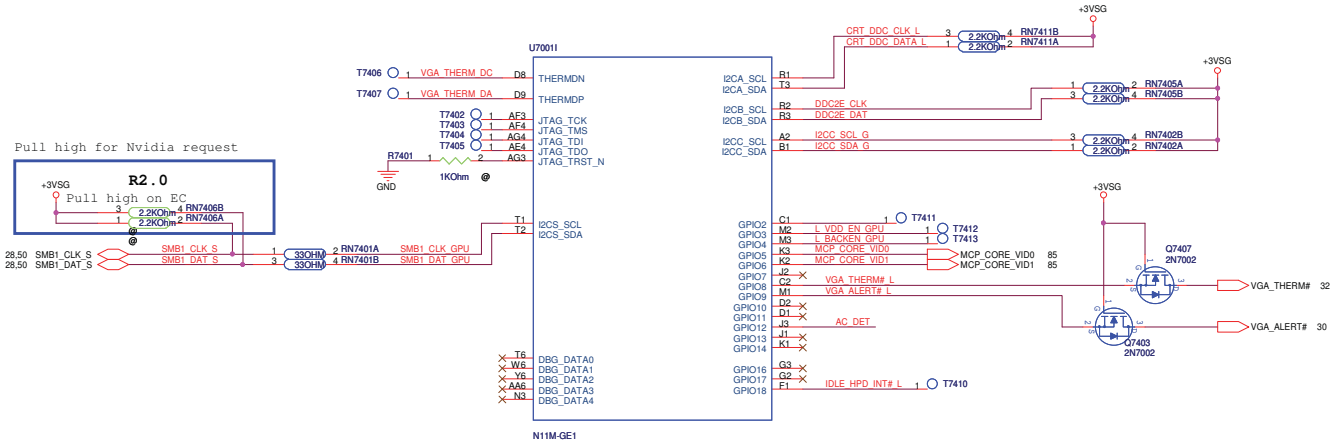
GPIO

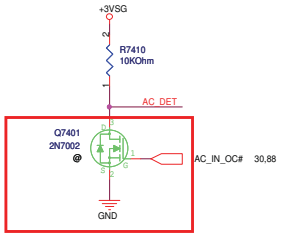
External thermal sensor

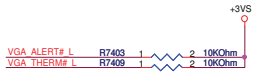
Remove External Thermal Sensor

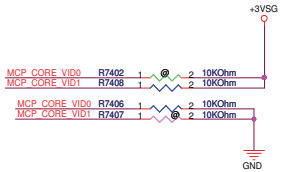
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	NVGEM
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD VID 0
6	OUT	HIGH	NVVDD VID 1
7	OUT	HIGH	FBVDD VID 0
8	IN/OUT	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	HIGH	FBVREF SELECT
11	OUT	HIGH	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL 0
14	OUT	HIGH	PS CONTROL 1









N10P-GE1 (N51VF)

GPU_VID_0	+VGA_VCORE_O
L	0.9V
H	1.1V

N10M-GS (N53)

GPU_VID_1	GPU_VID_0	+VGA_VCORE_O
H	L	1.0V
L	H	0.85V
L	L	0.8V

GPU_VID0	GPU_VID1	+VGA_VCORE
H	H	
H	L	1V
L	H	0.85V
L	L	0.8V

ASUSTeK COMPUTER INC.

Title : N10M-GE1 (5)

Engineer: Leon

Size	Project Name	Rev
C	U35JC	1.0

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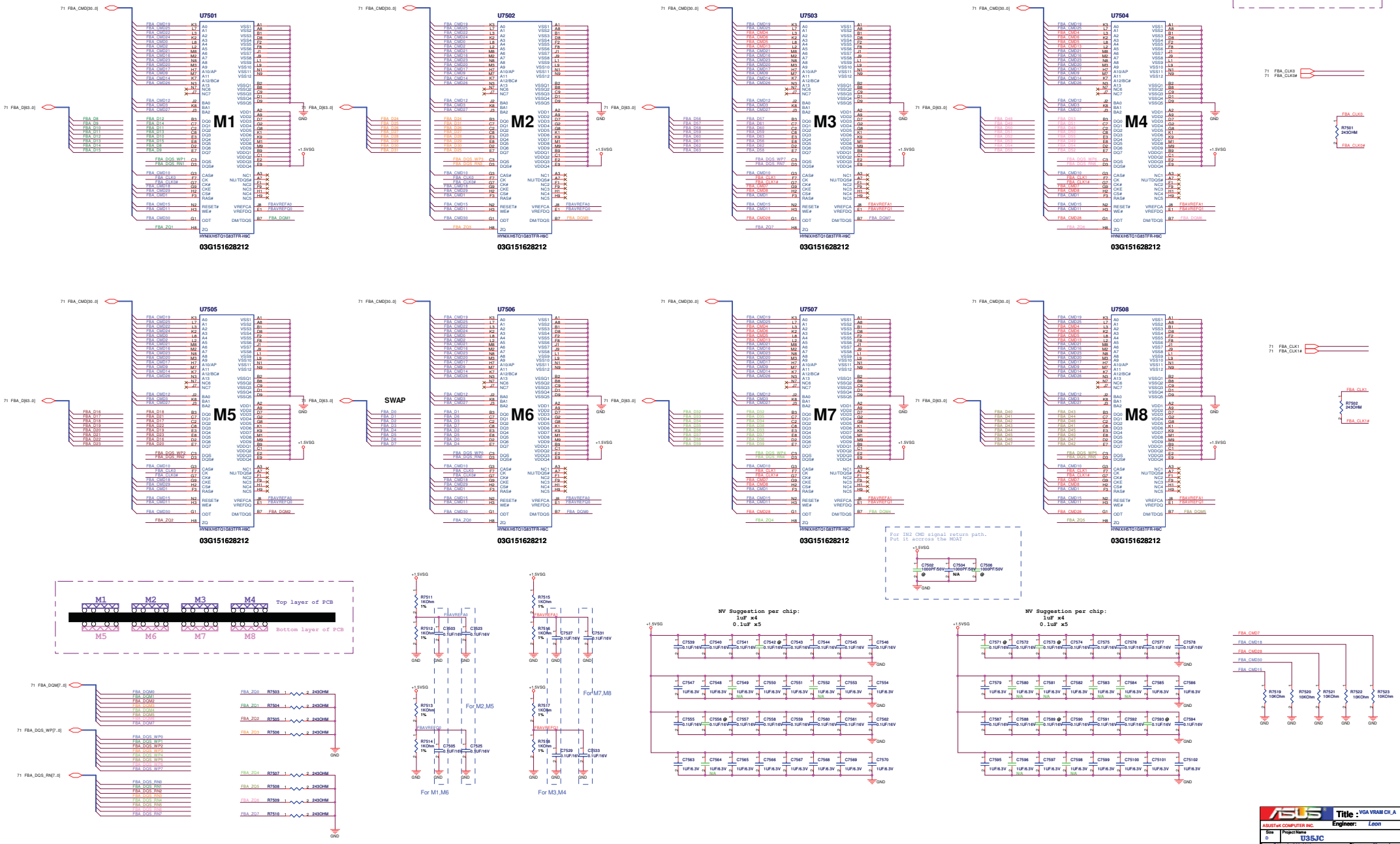
Second Source P/N:
1. 03G151628211 (Hynix)
2. 03G151628320 (Samsung)



ASUSTeK COMPUTER INC.

Title : VGA VRAM CH_A

Engineer: Leon

Size	Project Name	Rev
D	U35JC	1.0

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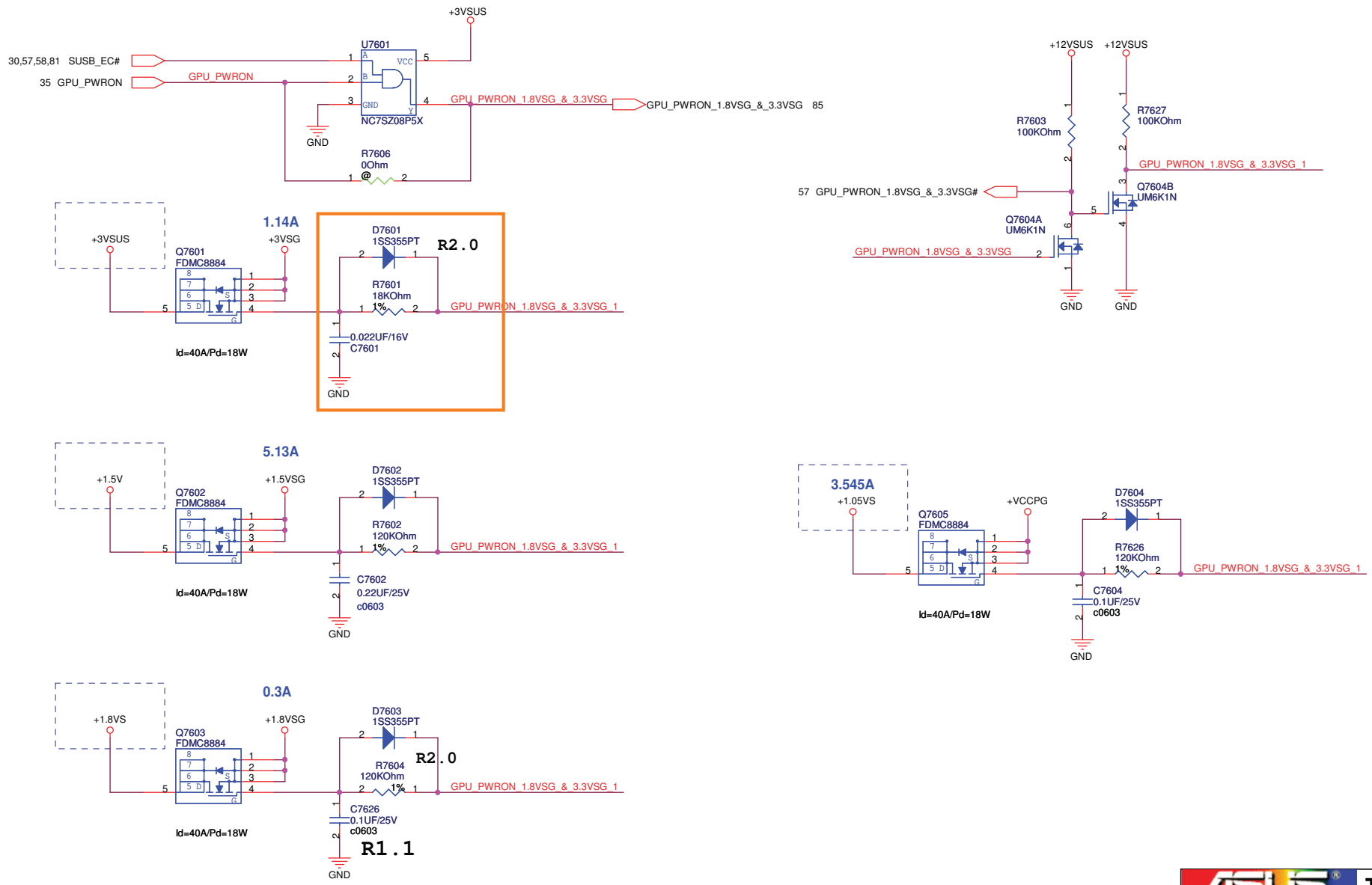

ASUSTeK COMPUTER INC.	Title : VGA Power Sequence	
	Engineer: Leon	
Size B	Project Name U35JC	Rev 1.0
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Title <Title>		
Size A	Document Number U35JC	Rev 1.0
Date: Tuesday, March 02, 2010	Sheet 77 of 99	

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ASUSTeK COMPUTER INC.	Title : <Title>	Engineer: Leon
Size: C	Project Name: U35JC	Rev: 1.0
Date: Tuesday, March 02, 2010	Sheet 78 of 99	

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ASUSTeK COMPUTER INC.	Title : <Title>	Engineer: Leon
Size: C	Project Name: U35JC	Rev: 1.0
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IMVP6.5 CPU VCORE REGULATOR

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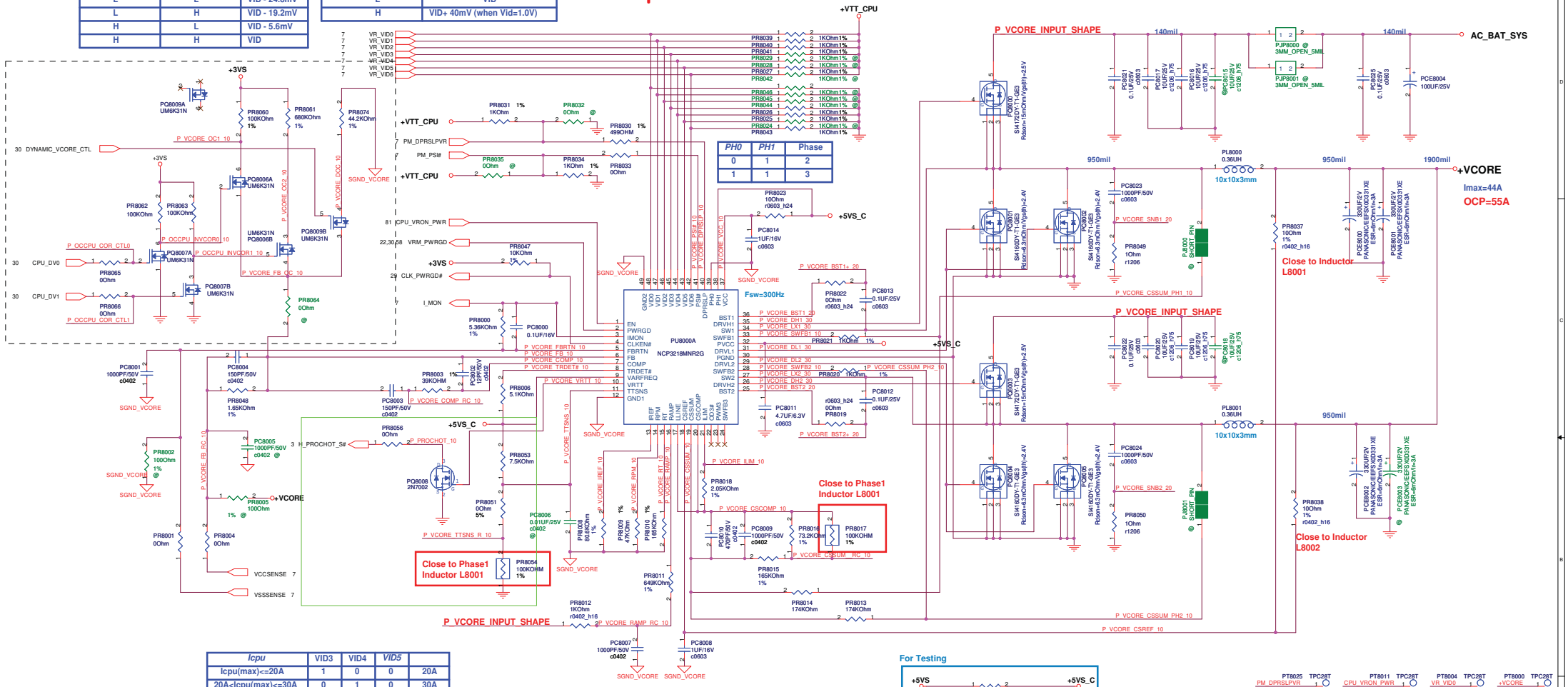
CPU_DV0	CPU_DV1	+VCORE
L	L	VID - 24.8mV
L	H	VID - 19.2mV
H	L	VID - 5.6mV
H	H	VID

DYNAMIC_VCORE_DV	+VCORE
L	VID
H	VID+ 40mV (when Vid=1.0V)

PH0	PH1	Phase
0	1	2
1	1	3

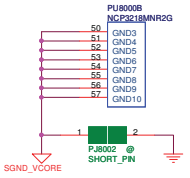


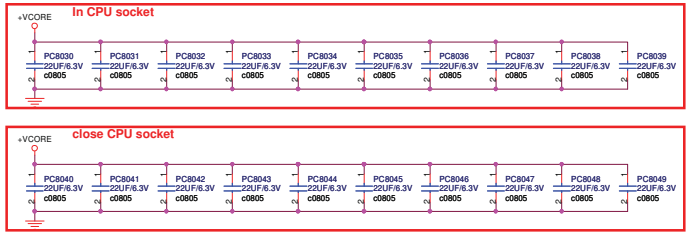
Icpu	VID3	VID4	VID5	
Icpu(max)<=20A	1	0	0	20A
20A<Icpu(max)<=30A	0	1	0	30A
30A<Icpu(max)<=40A	1	1	0	40A
40A<Icpu(max)<=50A	0	0	1	50A
50A<Icpu(max)<=60A	1	0	1	60A
60A<Icpu(max)<=70A	0	1	1	70A
70A<Icpu(max)<=90A	1	1	1	90A

ARD 35W
CFD 45W

CPU Spec	MAX. current	OCP setting	PR8018
45W(CFD)	52A	65A	2.05Kohm
35W(ARD)	48A	55A	1.74Kohm

CPU Spec	MAX. current	PR8000(I_mon)
35W(ARD)	50A	5.43K ohm
45W(CFD)	60A	5.36Kohm





PT8025 TPC28T PM_DPRSLPVR	PT8011 TPC28T CPU_VRON_PWR	PT8004 TPC28T VR_VID0	PT8000 TPC28T +VCORE
PT8026 TPC28T CPU_DV0	PT8012 TPC28T CLK_PWRGD#	PT8005 TPC28T VR_VID1	PT8001 TPC28T +VCORE
PT8024 TPC28T CPU_DV1	PT8013 TPC28T VRM_PWRGD	PT8006 TPC28T VR_VID2	PT8002 TPC28T +VCORE
PT8023 TPC28T H_PROCHOT_S#	PT8014 TPC28T I_MON	PT8007 TPC28T VR_VID3	PT8003 TPC28T +VCORE
PT8027 TPC28T PM_PS#	PT8015 TPC28T VCCSENSE	PT8008 TPC28T VR_VID4	PT8018 TPC28T GND
	PT8016 TPC28T VSSSENSE	PT8009 TPC28T VR_VID5	PT8019 TPC28T GND
	PT8017 TPC28T +5VS_C	PT8010 TPC28T VR_VID6	PT8020 TPC28T GND
			PT8021 TPC28T GND

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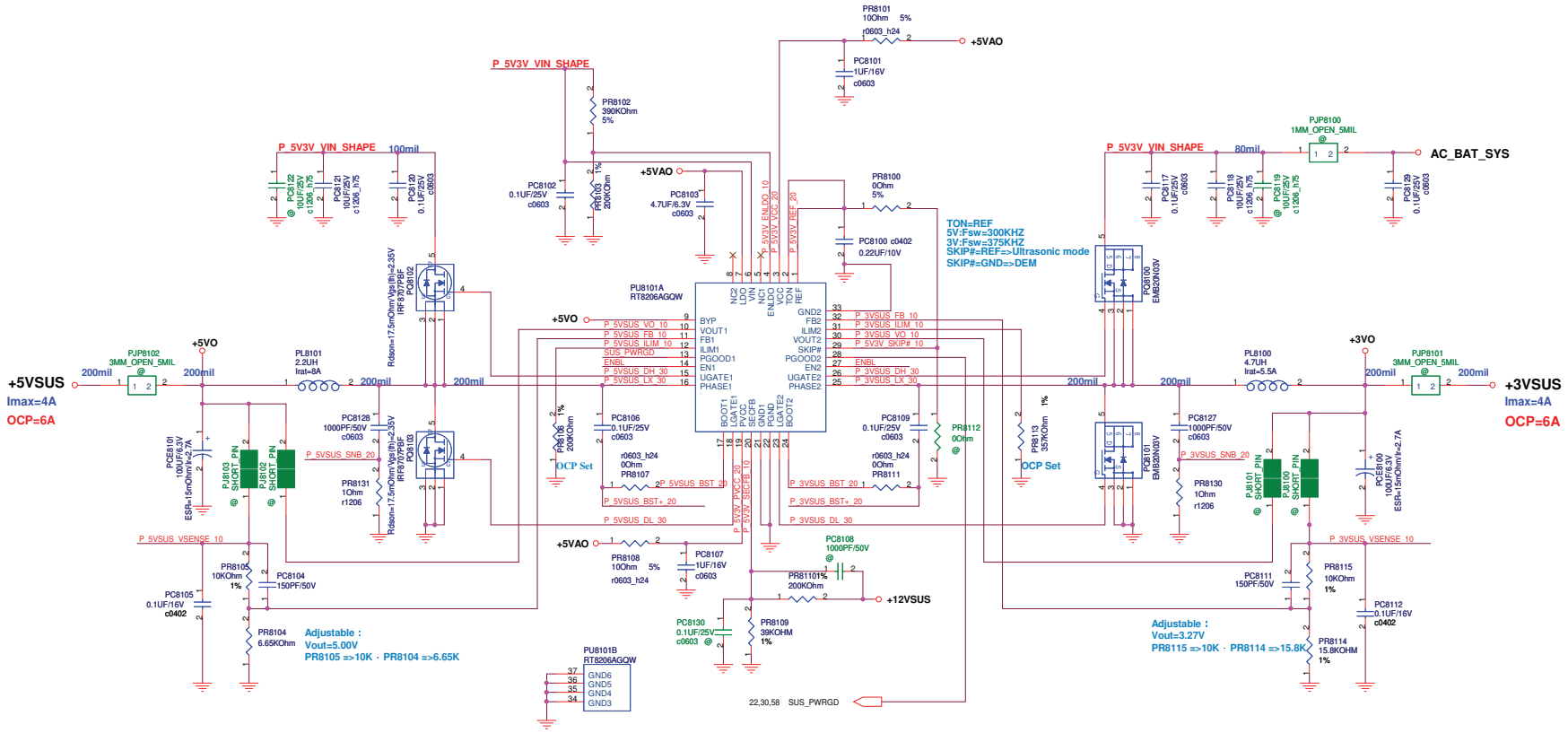
+5VSUS / +3VSUS POWER SUPPLY



Power stage

+5VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.96A
2. Ripple Current:
   Irip=2.61A
3. Ripple Voltage:
   ESR/1=45mohm
   V=117.45mV
4. Inductor Spec:
   Isat=6.2A
   Idc=4.6A
   DCR=36mohm
5. MOSFET Spec:
   H-side MOSFET: FDMC8884
   Rds(ON)=30mohm (Vgs=4.5 V)
   I cont = 9A (T =25 ℃)
   I peak =15A (Pause =10 us)
   L-side MOSFET: FDMC8884
   Rds(ON)=30mohm (Vgs=4.5 V)
   I cont = 9A (T =25 ℃)
   I peak =15A (Pause =10 us)

+3VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.96A
2. Ripple Current:
   Irip=1.55A
3. Ripple Voltage:
   ESR/1=45mohm
   V=69.75mV
4. Inductor Spec:
   Isat=6.2A
   Idc=4.6A
   DCR=36mohm

Controller

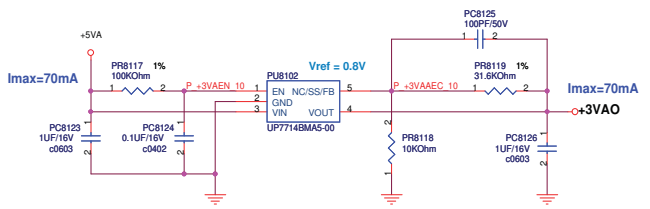
+5VSUS:

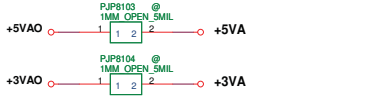
1. Voltage & Current:
   +5VSUS: 5V / 4A
2. Frequency:
   F=300KHZ
3. OCP:
   Set R8116=357 Kohm
   Iocp=5uA*Rocp/10*Rds(on)
   Iocp=6A
4. Soft start time:
   The Soft Start duration is 2ms
5. Inrush Current:
   C total = 100 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.25 A

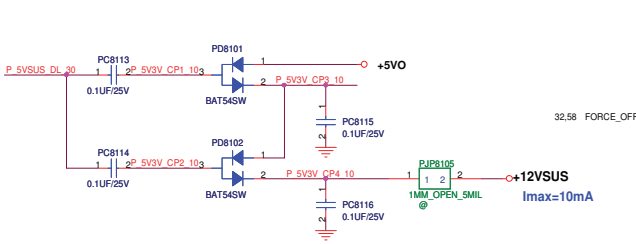
+3.VSUS

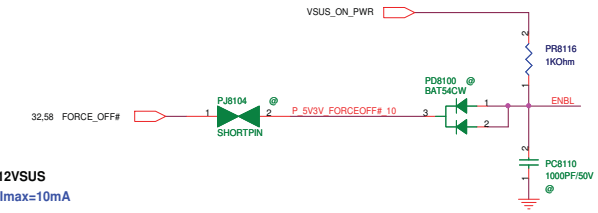
1. Voltage&Current:
   +3VSUS: 3.3V / 4A
2. Frequency:
   F=375KHZ
3. OCP:
   Set R8109=357KOhm
   Iocp=5uA*Rocp/10*Rds(on)
   Iocp=6A
4. Inrush Current:
   C total = 100 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.165 A

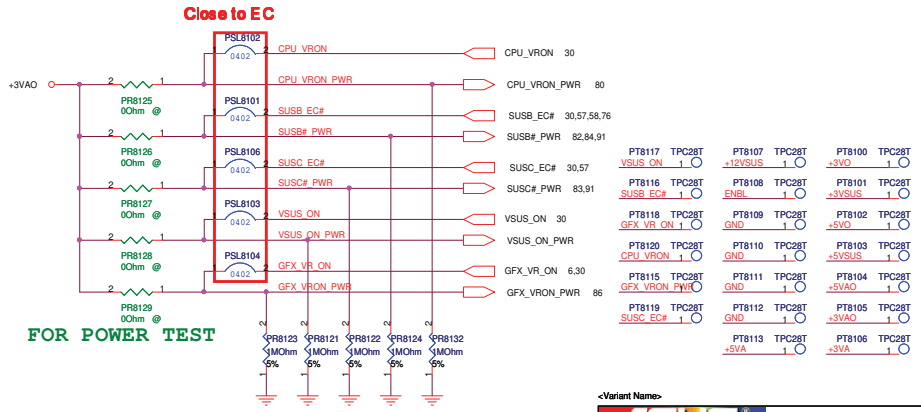
+3VAO











Can delete pull down R when EC have pull low R(Page 30)

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_SYSTEM	
	Engineer: Morris/Sting	
Size: Custom	Project Name: U35JC	Rev: 2.00
Date: Friday, April 09, 2010	Sheet 81 of 99	

+VTT_CPU & +VTT_PCH & +1.05VS POWER SUPPLY

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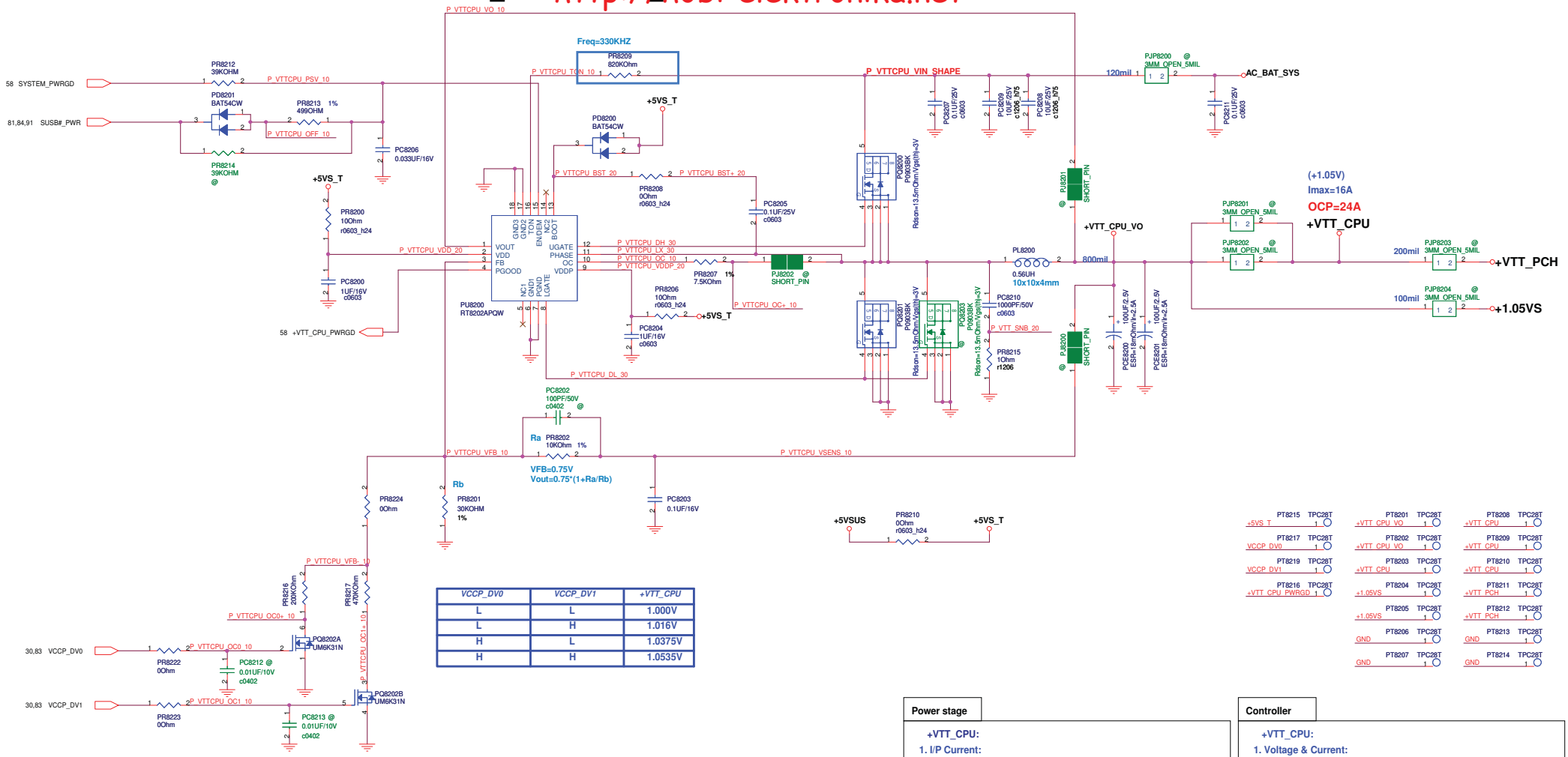

VCCP_DV0	VCCP_DV1	+VTT_CPU
L	L	1.000V
L	H	1.016V
H	L	1.0375V
H	H	1.0535V

Power stage

+VTT_CPU:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.33A
2. Ripple Current:
   Irip=9.18A
3. Ripple Voltage:
   ESR/2=7.5mohm
   V=68.85mV
4. Inductor Spec:
   Isat=29.1A
   Idc=26A
   DCR=1mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0353DPA

   Rds(ON)=7.6mohm (Vgs=4.5 V)
   I cont = 35A (T =25 ℃)
   I peak =140 A (Pause =10 us)

Controller

+VTT_CPU:

1. Voltage & Current:
   +VTT_CPU: 1.05V / 15A
2. Frequency:
   F=300KHZ
3. OCP:
   Set R8202=4.99 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=26A
4. Soft start time:
   The SS duration is 1.35ms
5. Inrush Current:
   C total = 440 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.342 A

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_+VTT	
	Engineer: Morris/Sting	
Size: Custom	Project Name: U35JC	Rev: 2.00
Date: Friday, April 09, 2010	Sheet 82 of 99	

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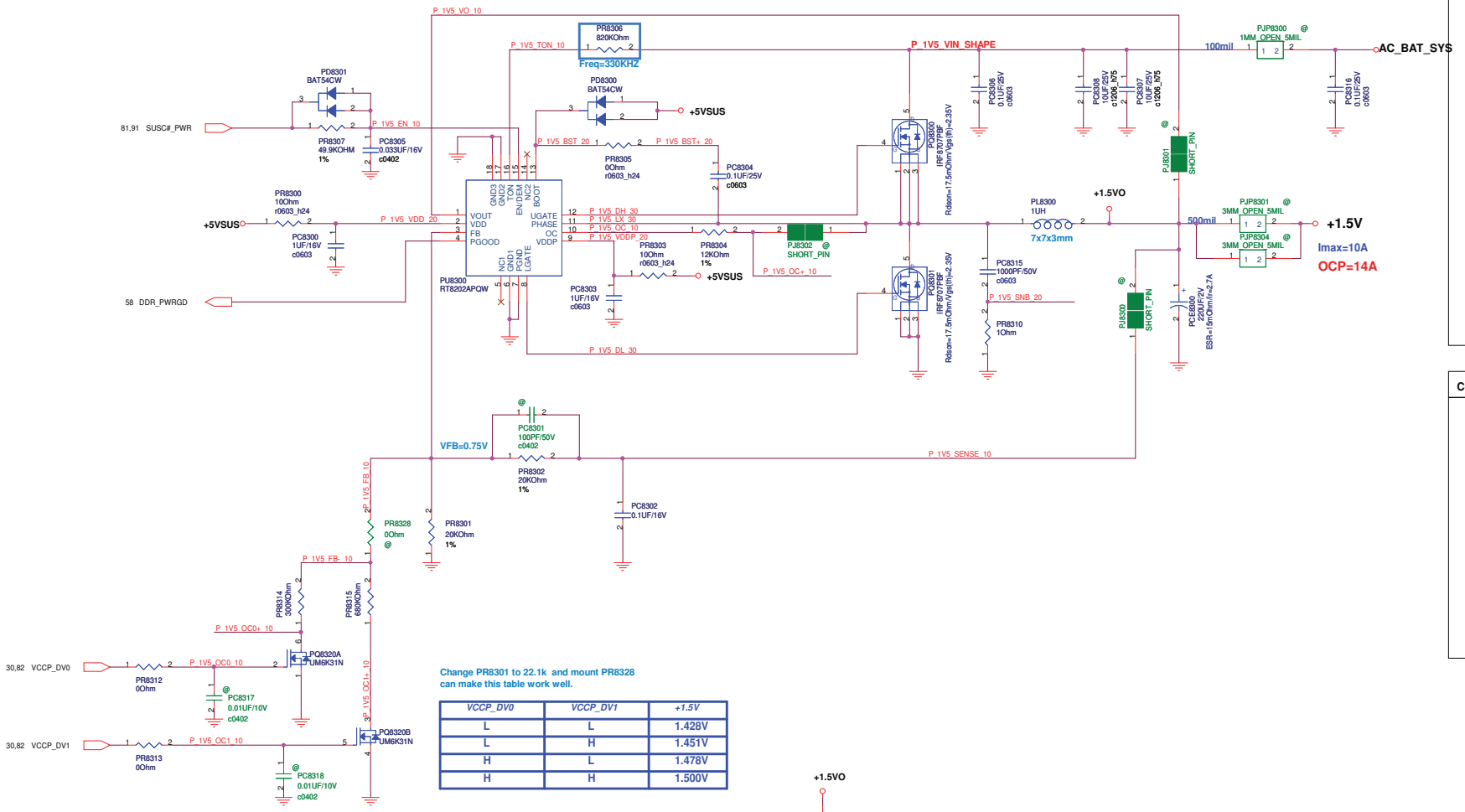
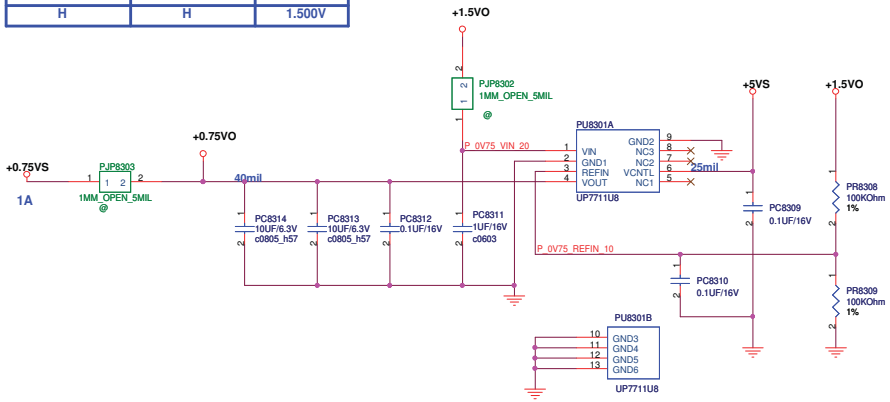
+1.5V & +0.75VS POWER SUPPLY



Change PR8301 to 22.1k and mount PR8328 can make this table work well.

VCCP_DV0	VCCP_DV1	+1.5V
L	L	1.428V
L	H	1.451V
H	L	1.478V
H	H	1.500V



Power stage

DDR III:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.22A
2. Ripple Current:
   Irip=4.62A
3. Ripple Voltage:
   ESR/1=15mohm
   V=69.3mV
4. Inductor Spec:
   Isat=12.7A
   Idc=9.5A
   DCR=8.5mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

Controller

DDR III:

1. Voltage & Current:
   +1.5V: 1.5V / 10A
2. Frequency:
   F=300KHZ
3. OCP:
   Set R8302=12 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=14.3A
4. Soft start time:
   The Soft Start duration is 1.35ms
5. Inrush Current:
   C total = 220 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.244 A

1. Voltage & Current:
   +0.75V: 0.75V / 1A

PT8300	TPC28T	+1.5VO
PT8301	TPC28T	+1.5VO
PT8302	TPC28T	+1.5V
PT8303	TPC28T	+1.5V
PT8304	TPC28T	+0.75VO
PT8305	TPC28T	+0.75VS
PT8306	TPC28T	GND
PT8307	TPC28T	GND
PT8308	TPC28T	GND
PT8309	TPC28T	GND

<Variant Name>

ASUS

Title : POWER_I/O_DDR

ASUSTeK COMPUTER INC. NB

Engineer: Morris/Sting

Size	Project Name	Rev
Custom	U35JC	2.00

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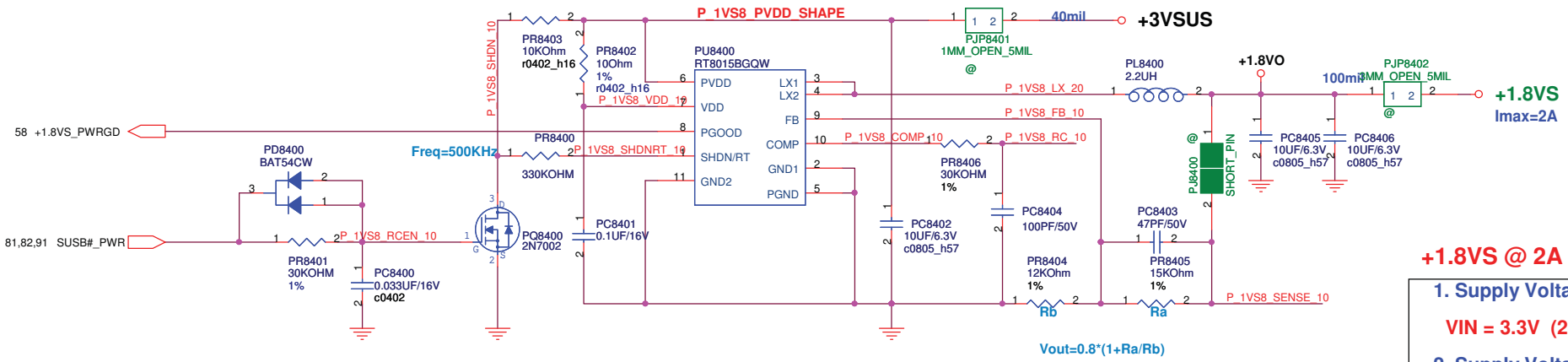
+1.8VS POWER SUPPLY



PT8404 TPC28T
+1.8VS_PWRGD 1

PT8400 TPC28T
+1.8VO 1

PT8401 TPC28T
+1.8VS 1

PT8402 TPC28T
GND 1

PT8403 TPC28T
GND 1

+1.8VS @ 2A

1. Supply Voltage:
   VIN = 3.3V (2.6V ~ 5.5V)
2. Supply Voltage:
   VOUT = 1.8V / 2A
3. Current Limit:
   I limit =3.2A
4. Continue Current:
   I cont = 1A
5. Feedback Voltage:
   VFB = 0.8V
6. Switching Frequency:
   Rrt = 330 Kohm
   Fsw =1000KHz

<Variant Name>

ASUS	Title : POWER_I/O_+1.8VS	
ASUSTeK COMPUTER INC. NB	Engineer: Morris/Sting	
Size: B	Project Name: U35JC	Rev: 2.00
Date: Friday, April 09, 2010	Sheet 84 of 99	

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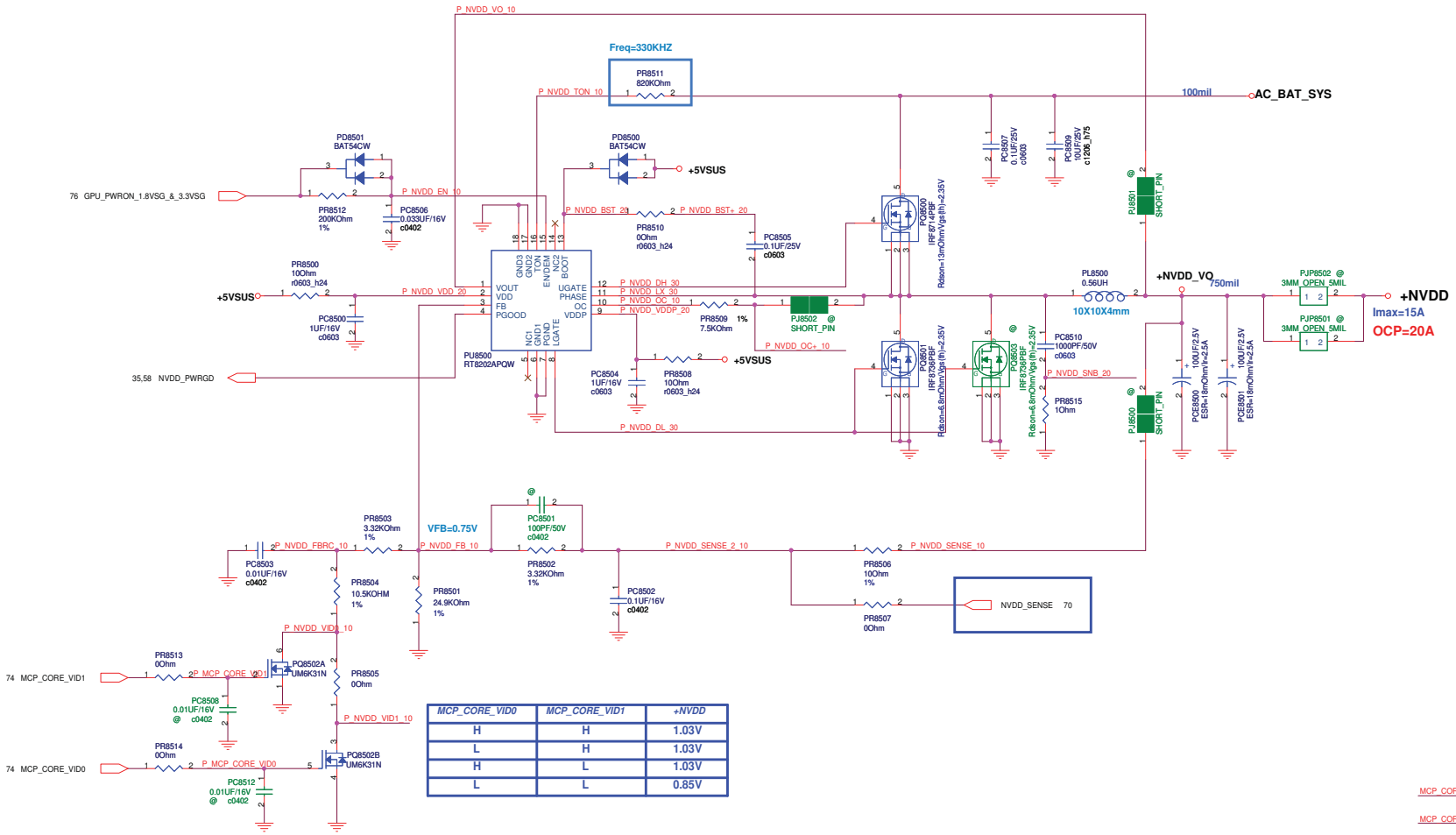
GPU NVDD POWER SUPPLY



MCP_CORE_VID0	MCP_CORE_VID1	+NVDD
H	H	1.03V
L	H	1.03V
H	L	1.03V
L	L	0.85V

Power stage

NVDD:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.11A
2. Ripple Current:
   Irip=6.4A
3. Ripple Voltage:
   ESR/2=7.5mohm
   V=48mV
4. Inductor Spec:
   Isat=26A
   Idc=17.5A
   DCR=4.2mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0353DPA

   Rds(ON)=7.6mohm (Vgs=4.5 V)
   I cont = 35A (T =25 ℃)
   I peak =140 A (Pause =10 us)

Controller

NVDD:

1. Voltage & Current:
   +NVDD: 0.95V / 15A
2. Frequency:
   F=300KHZ
3. OCP:
   Set R8504=7.5 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=20A
4. Soft start time:
   The Soft Start duration is 1.35ms
5. Inrush Current:
   C total = 440 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.310 A

MCP_CORE_VID0	PT8511	TPC28T	+NVDD	PT8503	TPC28T
MCP_CORE_VID1	PT8513	TPC28T	+NVDD	PT8504	TPC28T
GPU_PWRON_1.8VSG_&_3.3VSG	PT8510	TPC28T	+NVDD	PT8500	TPC28T
NVDD_PWRGD	PT8509	TPC28T	+NVDD_VO	PT8507	TPC28T
NVDD_SENSE	PT8512	TPC28T	+NVDD_VO	PT8508	TPC28T
			GND	PT8501	TPC28T
			GND	PT8502	TPC28T
			GND	PT8505	TPC28T
			GND	PT8506	TPC28T

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : POWER_I/O_NVDD

Engineer: Morris/Sting

Size	Project Name	Rev
Custom	U35JC	2.00

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RENDER CORE POWER SUPPLY

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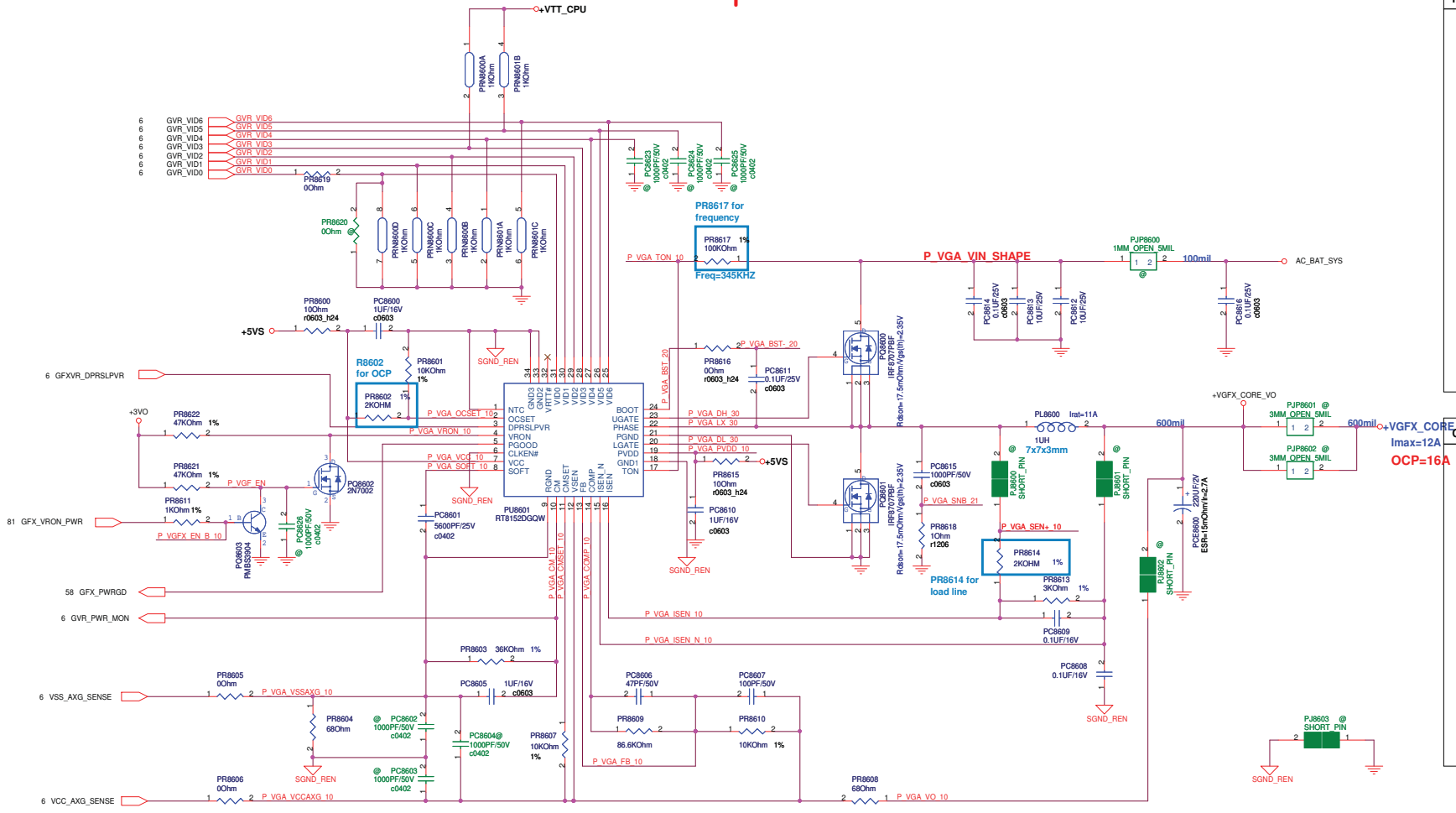

Power stage

+VGFX:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.22A
2. Ripple Current:
   Irip=7.28A
3. Ripple Voltage:
   ESR/2=7.5mohm
   V=54.6mV
4. Inductor Spec:
   Isat=26A
   Idc=17.5A
   DCR=4.2mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0353DPA

   Rds(ON)=7.6mohm (Vgs=4.5 V)
   I cont = 35A (T =25 ℃)
   I peak =140 A (Pause =10 us)

Controller

+VGFX:

1. Voltage & Current:
   +VGFX: 1V / 15A
2. Frequency:
   Ton=241nS
   Rton=150kohm
   Fsw=277KHZ
3. OCP:
   Vocset=VCC*R8612/(R8602+R8612)= 3.844V
   Imax= Vocset/(40*DCR)=21A
4. Soft start time:
   The Soft Start duration is 0.75ms(Css=10nF, SOFT=1.5V)
5. Inrush Current:
   C total = 440 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.587 A
6. LoadLine:
   DROOP=7mohm

PT8623	TPC28T VSS_AXG_SENSE	PT8603	TPC28T +VGFX_CORE		
PT8625	TPC28T VCC_AXG_SENSE	PT8604	TPC28T +VGFX_CORE		
PT8621	TPC28T GFX_PWRGD	PT8600	TPC28T +VGFX_CORE		
PT8626	TPC28T GVR_PWR_MON	PT8609	TPC28T +VGFX_CORE_VO	PT8610	TPC28T GVR_VID0
PT8619	TPC28T P_VGF_EN	PT8602	TPC28T +VGFX_CORE_VO	PT8611	TPC28T GVR_VID1
PT8617	TPC28T P_VGFX_EN_B_10	PT8601	TPC28T +VGFX_CORE_VO	PT8612	TPC28T GVR_VID2
PT8620	TPC28T GFX_VRON_PWR	PT8606	TPC28T GND	PT8613	TPC28T GVR_VID3
PT8622	TPC28T GFXVR_DPRSLPVR	PT8605	TPC28T GND	PT8614	TPC28T GVR_VID4
		PT8607	TPC28T GND	PT8615	TPC28T GVR_VID5
		PT8608	TPC28T GND	PT8616	TPC28T GVR_VID6

<Variant Name>

ASUS	Title : POWER_+VGFX_CORE	
<OrgName>	Engineer: Morris/Sting	
Size: Custom	Project Name: U35JC	Rev: 2.00
Date: Friday, April 09, 2010	Sheet 86 of 99	

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<Variant Name>

ASUS	Title :	
<OrgName>	Engineer:	
Size: Custom	Project Name	Rev: 1.1
Date: Friday, April 09, 2010	Sheet 87 of 99	

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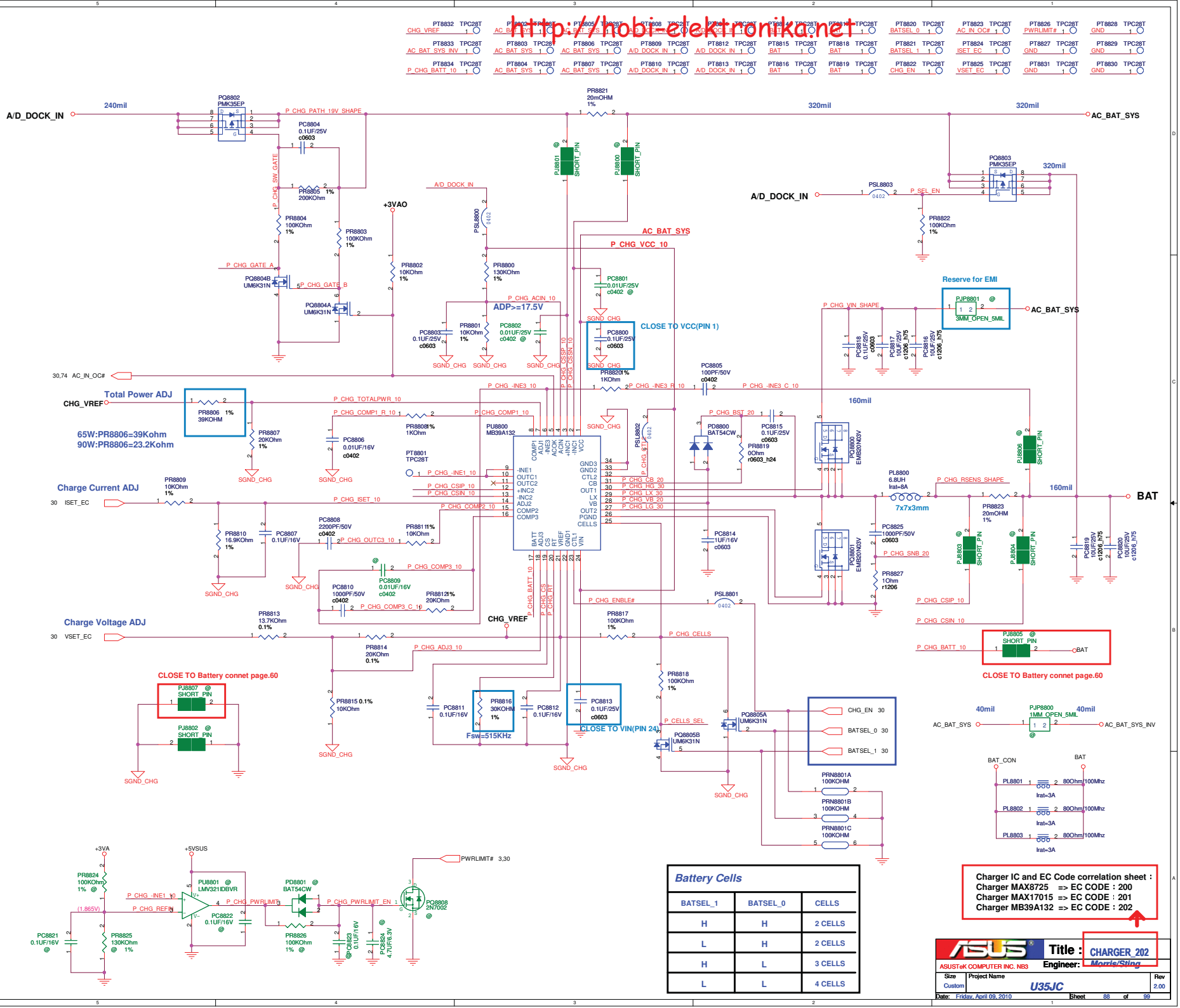

Battery Cells

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202

ASUSTeK COMPUTER INC. NB3

Title : CHARGER_202

Engineer: Morris/Sting

Size	Project Name	Rev
Custom	U35JC	2.00

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<Variant Name>

ASUS	Title :	
<OrgName>	Engineer:	
Size: Custom	Project Name	Rev: 1.1
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<Variant Name>

ASUSTeK COMPUTER INC. NB	Title :	
	Engineer:	
Size: Custom	Project Name	Rev: 1.1
Date: Friday, April 09, 2010	Sheet 90 of 99	

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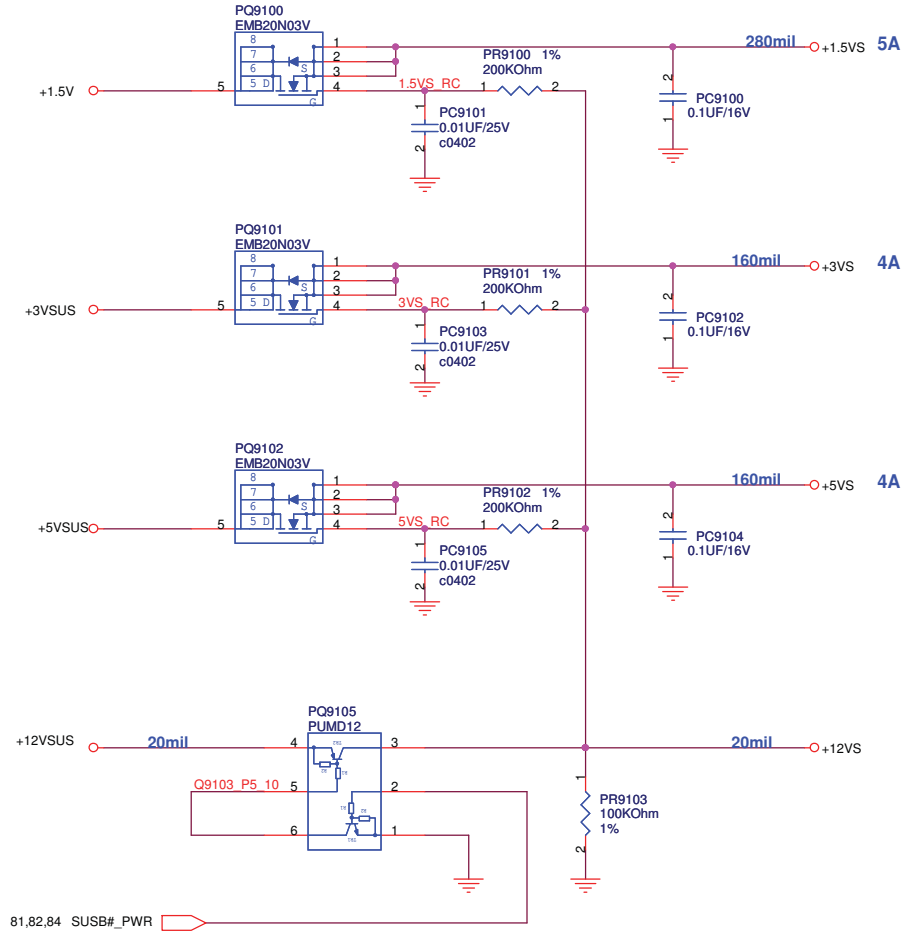
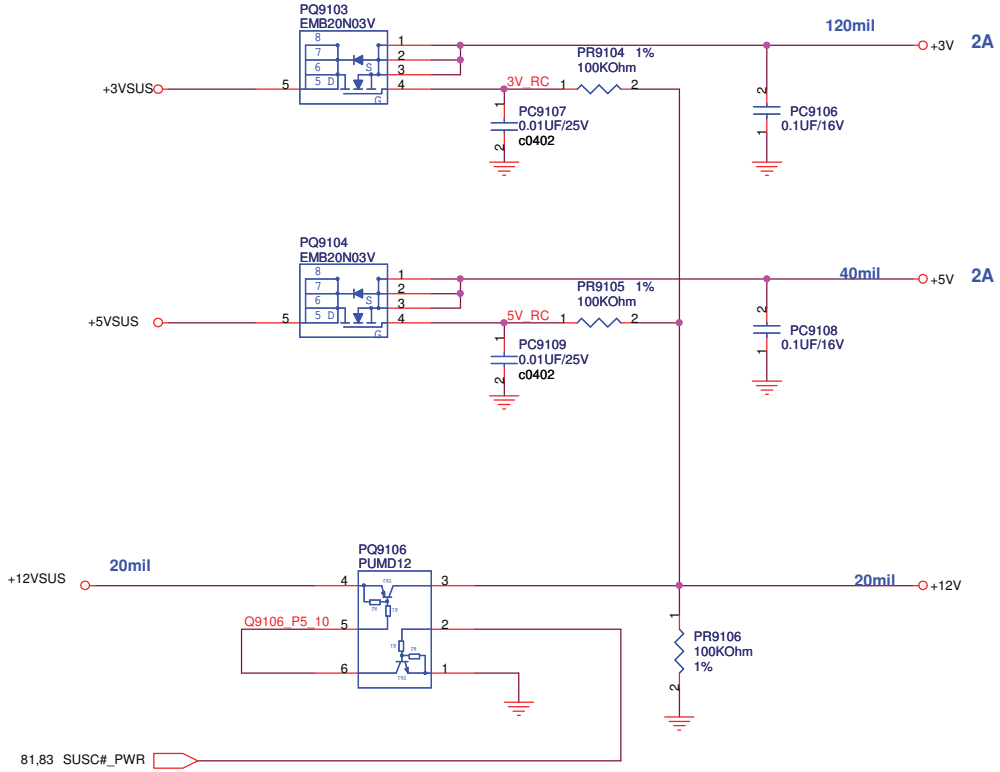
SUSB#_PWR POWER



SUSC#_PWR POWER



PT9100	TPC28T	PT9104	TPC28T
+1.5VS	1	+3V	1
PT9101	TPC28T	PT9105	TPC28T
+3VS	1	+5V	1
PT9102	TPC28T	PT9106	TPC28T
+5VS	1	+12V	1
PT9103	TPC28T		
+12VS	1		

Total count: 27 pcs

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_LOAD SWITCH

Engineer: Morris/Sting

Size	Project Name	Rev
B	U35JC	2.00

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Title <Title>		
Size A	Document Number U33JC	Rev 1.1
Date: Friday, April 09, 2010	Sheet 92 of 99	

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AC_BAT_SYS	AC_BAT_SYS	80,81,82,83,85,86,88
BAT	BAT	88
+3VAO	+3VAO	81,88
+5VA	+5VA	81
+3VA	+3VA	20,30,57,60,62,63,81,88,97
+5VAO	+5VAO	81
+5VO	+5VO	81
+5VSUS	+5VSUS	27,31,62,63,81,82,83,85,88,91
+5V	+5V	18,52,57,62,63,91,97
+5VS	+5VS	27,30,31,46,48,50,51,57,62,63,80,83,86,91,97
+3VO	+3VO	58,81,86
+3VSUS	+3VSUS	26,27,28,30,31,58,63,76,81,84,91
+3V	+3V	24,29,31,45,57,61,62,63,91
+3VS	+3VS	16,17,20,21,22,23,24,25,26,27,28,29,30,31,32,35,44,45,46,48,50,51,57,58,61,63,74,80,91,97
+12VSUS	+12VSUS	26,28,76,81,91
+12V	+12V	28,91
+12VS	+12VS	28,45,91
+1.8VO	+1.8VO	84
+1.8VS	+1.8VS	7,26,57,76,84
+0.75VS	+0.75VS	16,17,57,83
+0.75VO	+0.75VO	83
+1.5V	+1.5V	3,6,7,16,17,18,29,57,63,76,83,91,97
+1.5VO	+1.5VO	83
+1.5VS	+1.5VS	26,29,57,63,91
+NVDD	+NVDD	57,70,85,97
+NVDD_VO	+NVDD_VO	85
+VGFX_CORE	+VGFX_CORE	6,57,86
+VGFX_CORE_VO	+VGFX_CORE_VO	86
+VCORE	+VCORE	6,7,57,80,97
+1.05VS	+1.05VS	76,82
+VTT_PCH	+VTT_PCH	26,27,82,97
+VTT_CPU	+VTT_CPU	3,6,7,25,26,27,57,80,82,86,97
+VTT_CPU_VO	+VTT_CPU_VO	82,97
A/D_DOCK_IN	A/D_DOCK_IN	63,88
AC_BAT_SYS_INV	AC_BAT_SYS_INV	45,88

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_SIGNAL

Engineer: Morris/Sting

Size	Project Name	Rev
Custom	U33JC	1.1

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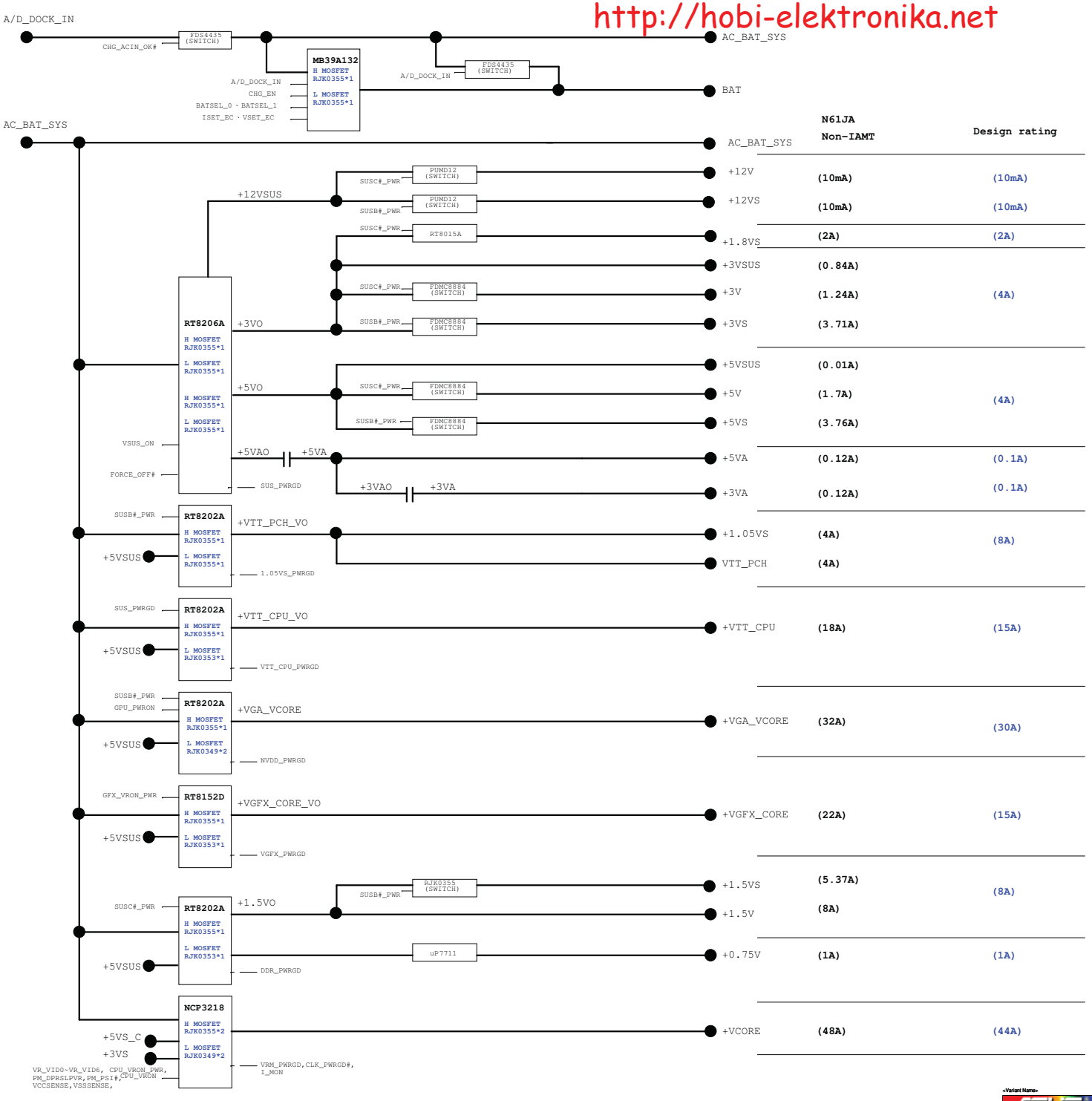

	N61JA Non-IAMT	Design rating
+12V	(10mA)	(10mA)
+12VS	(10mA)	(10mA)
+1.8VS	(2A)	(2A)
+3VSUS	(0.84A)	
+3V	(1.24A)	(4A)
+3VS	(3.71A)	
+5VSUS	(0.01A)	
+5V	(1.7A)	(4A)
+5VS	(3.76A)	
+5VA	(0.12A)	(0.1A)
+3VA	(0.12A)	(0.1A)
+1.05VS	(4A)	(8A)
VTT_PCH	(4A)	
+VTT_CPU	(18A)	(15A)
+VGA_VCORE	(32A)	(30A)
+VGFX_CORE	(22A)	(15A)
+1.5VS	(5.37A)	(8A)
+1.5V	(8A)	
+0.75V	(1A)	(1A)
+VCORE	(48A)	(44A)

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Rev	Date	Description
1.00	01/08 '2010	First Release!
1.10	01/20 '2010	01. Swap Debug Connect, page 44
		02. Modify circuit for AZWAVE/INTEL WiFi minicard, page 61
		03. Mount EDID resistor fro MODS, R3532, R3533, R3590, R3591, page 35
		04. Check Strap[0,1,2] setting for MP GPU, page 72
	01/22 '2010	05. Remove LVDS_GPU_SW/SW#, remove R3564, R3567, R3571, R3596, Q3552, page 35
		06. Change CPU_DV0/CPU_DV1 to GPJ4/GPJ5, page30
		07. Change VCCP_DV0/VCCP_DV1 to GPF2/GPF3, page30
		08. Change MARATHON# to GPE7, page30
	01/27 '2010	09. Change LVDS CONN, page45
		10. Check thermal sensor on PR, page50
		11. XTAL 14.318MHz C2913, C2914 to 18PF, page29
		12. Refer K72F to modify ICS9LVS3162B circuit, page 29
		13. XTAL 27MHz C7308, C7309 to 27PF, page73
		14.Change CLK_OC to Clock_select_uc, paage 30
		15.Change EC GPG2/GPG6 from CLK_STRAP[0,1] to T3019/T3020, paage 30
		16.Change EC GPE5 from CLK_OC to T3021, paage 30

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[M61JA] R1.0 => R1.1

1. Follow E.E RC delay
   +5v R9107 100K change to 68K
   +3v R9106 200K change to 121K
   +1.5v R8306 49.9K change to 68K
   +5VS R9104 200K change to 68K
   +3VS R9103 200K change to 121K
   +1.8VS R8401 33.2K change to 121K
   +1.5VS R9102 470K change to 390K
   +1.05VS R8252 39K change to 200K
   +0.75VS R8312 0 change to 2.49K C8310 0.1U change to 2.2U

2. VR_VID0~2 pull high 1K VR_VID6 pull low 1K.
3. U8401 RT8015A change to RT8015B
4. Reserve GVR_VID0~VID6 pull high and low resistor R8627~R8633
5. Reserve R8517~R5720 pull high & pull low risistor for MCP_CORE_VID
6. page86 component option change to ARD (CFD no stuff)
7. R8004 option change to CFD & R8049 change to ARD(For IMON)
8. Change RN8801A RN8801B(layout request)
9. R8517 R8519 change to stuff
10. R8406 13K change to 12K
11. CE8005 no stuff , CE8007 stuff
12. C8403 C8406 size 0603 change to 0805
13. R8213 R8305 ohm change to 2.2 ohm
14. R8621~R8633 stuff 1K ohm
15. R8512 change form 200K to 33K ohm
16. VTT_PCH component option change to CFD
17. Delete U8502 & GPU_PWRON signal change to GPU_PWRON_1.8VSG_&_3.3VSG
18. L8601 1uH => 0.56uH , C8608 0.01uF/50 => 0.01uF/16V , R8621 43K => 36K , C8617 =>0.1uF/16V 1uF/10V , C8607 68pF/50V => 33pF/50V , R8625 10K => 18.7K , R8613 3.6K => 4.02K
19. R8057 change form 10K to 2.05K
20. Add Q8007 & Q8008 form thermal issue

ASUS	Title : System History	
ASUSTeK COMPUTER INC. NB	Engineer:	
Size: Custom	Project Name: U35JC	Rev
Date: Friday, April 09, 2010	Sheet 96 of 99	

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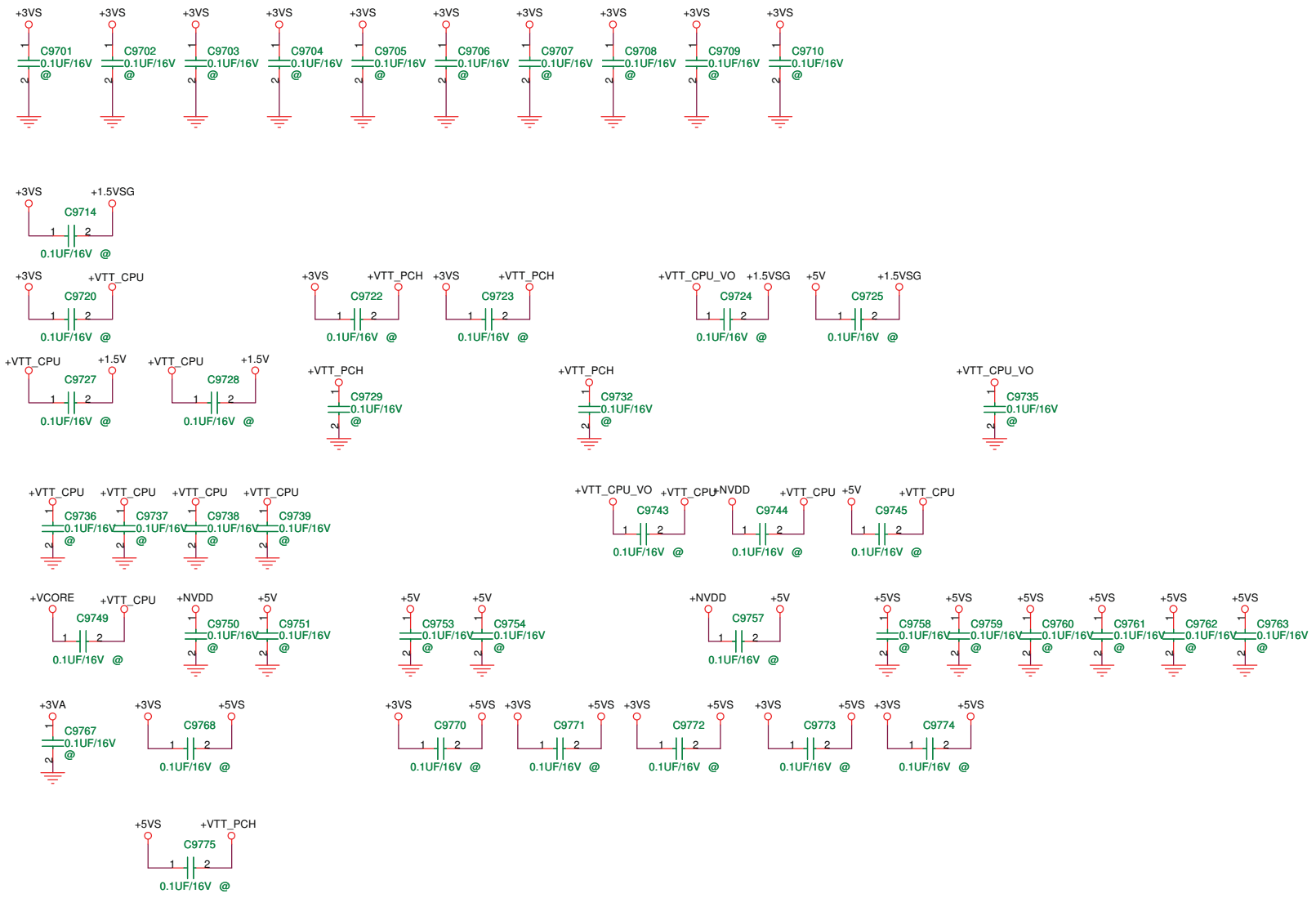

ASUSTeK COMPUTER INC. NB3	Title : OTH_EMI Caps	
	Engineer: Wendell_lo	
Size: B	Project Name: U35JC	Rev: 1.0
Date: Friday, April 09, 2010	Sheet 97 of 99	

AC-IN Mode

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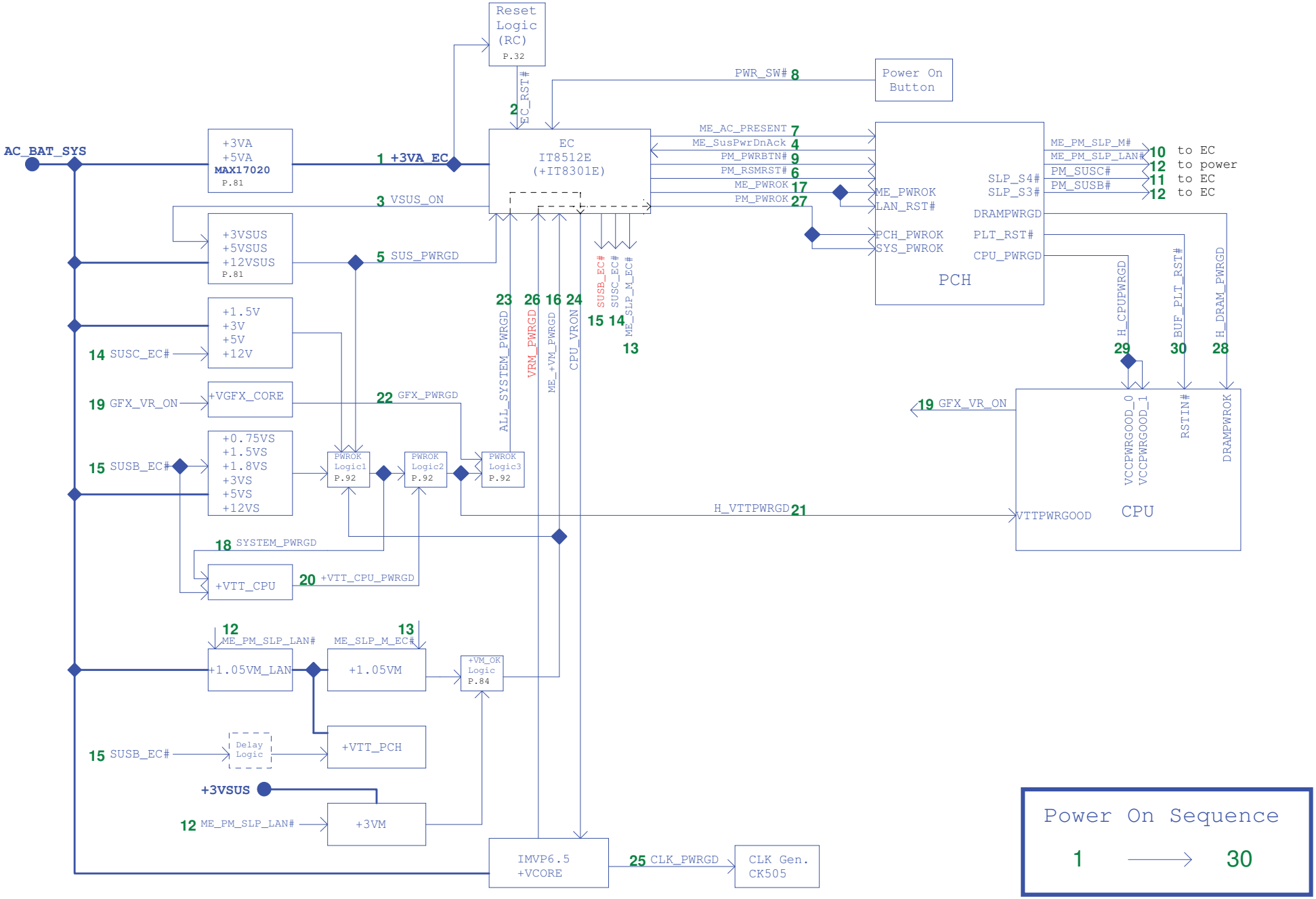
M52J Power On Sequence Diagram Rev. 0.31



ASUS ASUSTeK COMPUTER INC	Title : POWER SEQUENCE	Engineer: Wendell_lo
Size C	Project Name U35JC	Rev 1.0
Date: Friday, April 09, 2010	Sheet 98 of 99	

M52J Power-On Sequence Timing Diagram Rev.0.31

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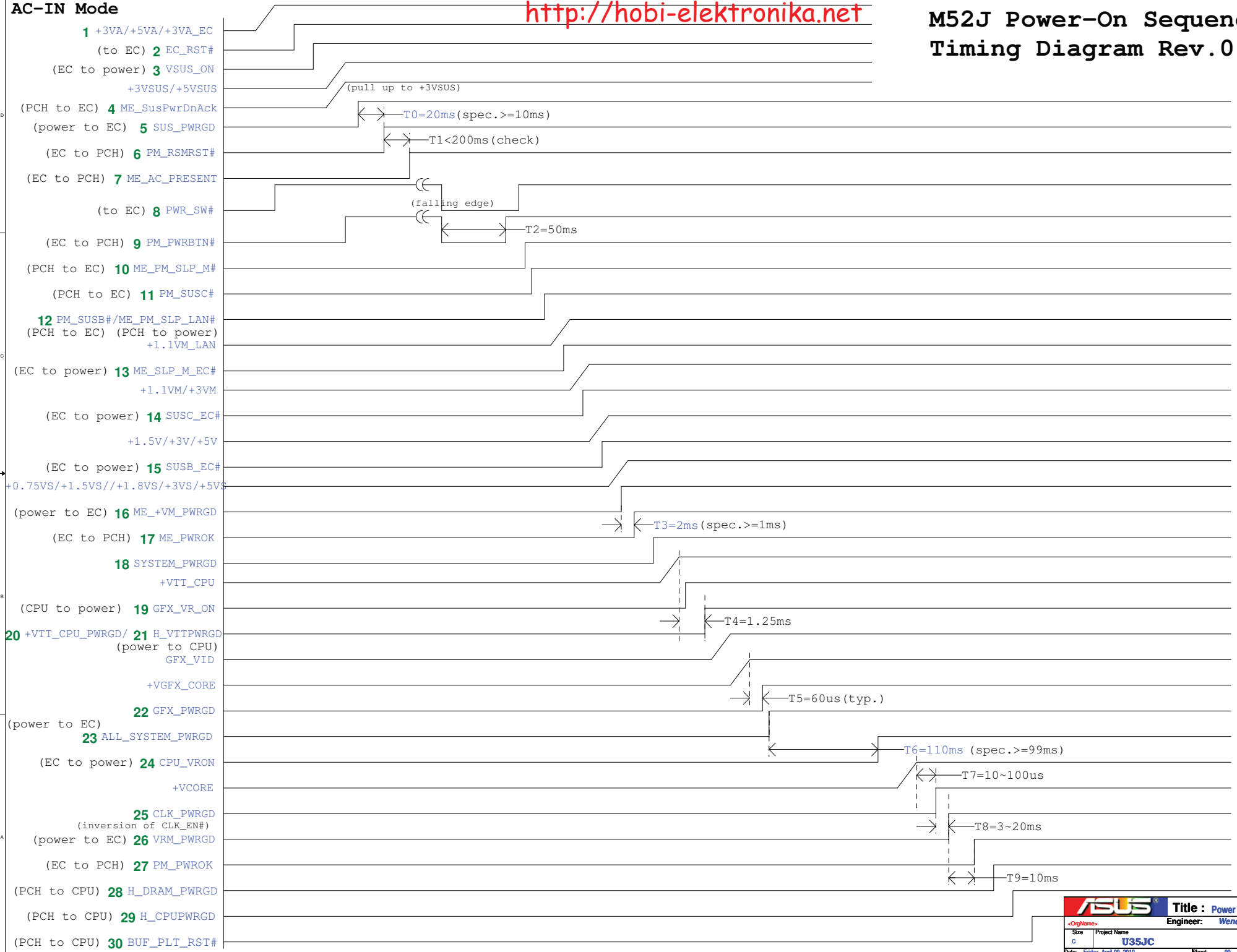
AC-IN Mode



ASUS	Title : Power On Timing		
<OrgName>	Engineer: Wendell_lo		
Size C	Project Name U35JC		Rev 1.0
Date: Friday, April 09, 2010	Sheet 99 of 99		